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HPCBS

High Performance Commercial Building Systems

IBECS Network/Ballast Interface - Final Report

Element 3 - Lighting, Envelope and Daylighting
Project 2.1 - Lighting Controls
Task 2.1.1 - Ballast Interfaces

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November, 2001

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Lawrence Berkeley National Laboratory Final Report

IBECS Network/Ballast Interface
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Executive Summary

This report describes the work performed to design, develop and demonstrate an IBECS network/ballast interface that is useful for economically controlling dimmable fluorescent lamp ballasts in commercial buildings. The first section of the report provides the general background of the IBECS (Integrated Building Environmental Communications System) research and development work as well as the context for the development of the network/ballast interface. The research and development effort that went into producing the first proof-of-concept circuit and the physical prototype of that concept is detailed in the second section. In the third section of the report, we describe the lessons learned from the first demonstration of the network/ballast interface in an office at LBNL. Electrical noise interference from the ballast encountered with the first generation of interface led to design changes that hardened the refined prototype from any electrical noise generated by the ballast. The final section of the report discusses the performance of refined prototype after we replaced the proof-of-concept prototype with the refined prototypes in the demonstration office at LBNL.

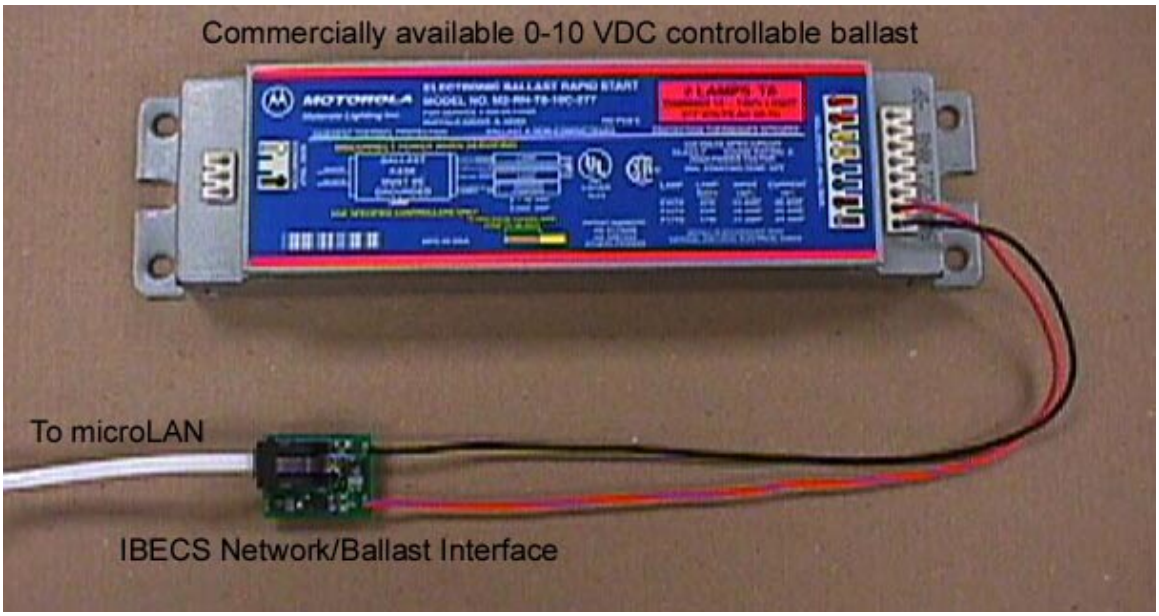

Figure i. Final IBECS network/ballast interface connected to a controllable ballast

We learned that newly available silicon microchips are a suitable platform for designing low-cost digital network/ballast interfaces that are useful for enabling network operation of commercially available 0-10 VDC dimming ballasts. We found that electrical noise generated by the ballast in the control loop can interfere with digital network operation unless the interface is hardened from this noise. We found that controllable ballasts from different companies generate different noise signatures. Using optical isolation, we produced a refined IBECS network/ballast interface that can provide universal control of most available 0-10 VDC controllable ballasts. In large quantities, we estimate that the cost of the universal interface would be about $1-2 to OEMs. This is 5 to 10 times cheaper per unit than any other proposed communications system.

Thus we successfully completed the task objectives by designing, developing, fabricating and demonstrating an IBECS network/ballast interface that is useful for economically dimming controllable ballasts.

IBECS Network/Ballast Interface
Final Report

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Introduction

This report describes the work performed to design, develop, and demonstrate an IBECS network/ballast interface that is useful for economically dimming controllable ballasts in commercial buildings. The first section of the report provides the general background of the IBECS (Integrated Building Environmental Communications System) research and development work as well as the context for the development of the network/ballast interface. The research and development effort that went into producing the first proof-of-concept circuit and the physical prototype of that concept is detailed in the second section. In the third section of the report, we describe the lessons learned from the first demonstration of the network/ballast interface at an office at LBNL. The fourth section describes how electrical noise interference encountered with the first generation of interface led to design changes for a refined prototype that hardened the interface from electrical noise generated by the ballast. The final section of the report discusses the performance of refined prototype after we replaced the proof-of-concept prototype with the refined prototypes in the demonstration office at LBNL.

Background

Lighting controls companies have developed controls products that can be specified as systems to achieve simple lighting control functions in buildings. Research conducted by LBNL in the late 1990s demonstrated that components from different manufacturers could be specified, assembled as systems, and installed in buildings to achieve simple lighting control functions and obtain significant energy savings. However, the fragmented nature of U.S. lighting controls market is such that manufacturers of lighting controls components (ballasts, switches and controls) produce products that often do not work well together as systems. Thus advanced lighting control equipment capable of implementing strategies such as daylighting proved difficult to commission in the field, leading to poor operation and user complaints. Failure to involve the occupants in the commissioning process also resulted in low occupant acceptance of more advanced lighting control strategies. The software that is necessary to coordinate the operation of lighting control sub-systems is also still immature and current systems lack appropriate networking software that would allow sub-systems from different manufacturers to communicate reliably.

To address the above market shortcomings, the overall technical goal IBECS Project is to develop an integrated building equipment communications (IBECS) network that will allow appropriate automation of lighting systems to increase energy efficiency, improve building performance, and enhance occupant experience in the space. This network will provide a low-cost means for occupants to control local lighting systems, thereby improving occupant comfort, satisfaction, and performance.

The goal of the IBECS project is to design, build, and test the IBECS interface and networking system between controllable lighting devices that will enable local and system-wide energy-efficient operations of various lighting systems and components.

IBECS Network/Ballast Interface Proof-of-Concept

The thrust of the IBECS work for FY2001 was to design, fabricate and demonstrate an IBECS network/ballast interface that is useful for economically dimming controllable ballasts from a digital network.

Any viable system for communicating with building lighting equipment should be able to accommodate the controllable ballasts currently available on the market. There are four dimming ballast types of interest for purposes of dimming lighting control in buildings:

- 0-10 VDC controllable ballasts (several companies manufacturing)
- Phase-cut (also called two-wire) ballasts (Advance Mark X is example)
- Three-wire ballasts (especially Lutron)
- Digital ballasts (only one company, Tridonic, currently producing in US)

The phase-cut ballasts, though less expensive than the other types of controllable ballasts, are not appropriate to widespread installation throughout a facility as the resulting harmonics introduced would negatively affect power quality. Three-wire ballasts, while of very high quality, cannot be dimmed using low-voltage circuits. Digital ballasts, though eventually the ideal vehicle for IBECS control, were thought to be a too limited market at this time. So for our initial interface development work, we elected to focus on the 0-10 VDC controllable ballasts.

How 0-10 VDC Controllable Ballasts Operate

At present, commercially available controllable (or dimming) ballasts for fluorescent lamps are equipped with two extra leads for controlling the intensity of the lamps. These extra leads form a two-wire low-voltage "bus," to which various control devices can be connected. For example, an appropriate photocell connected to the low-voltage "bus" can control the ballast light output by varying the voltage on the bus. It is common practice to connect several ballasts in parallel to the low-voltage bus so that multiple ballasts can be controlled in unison from a single controller or photocell (see **Figure 1**).

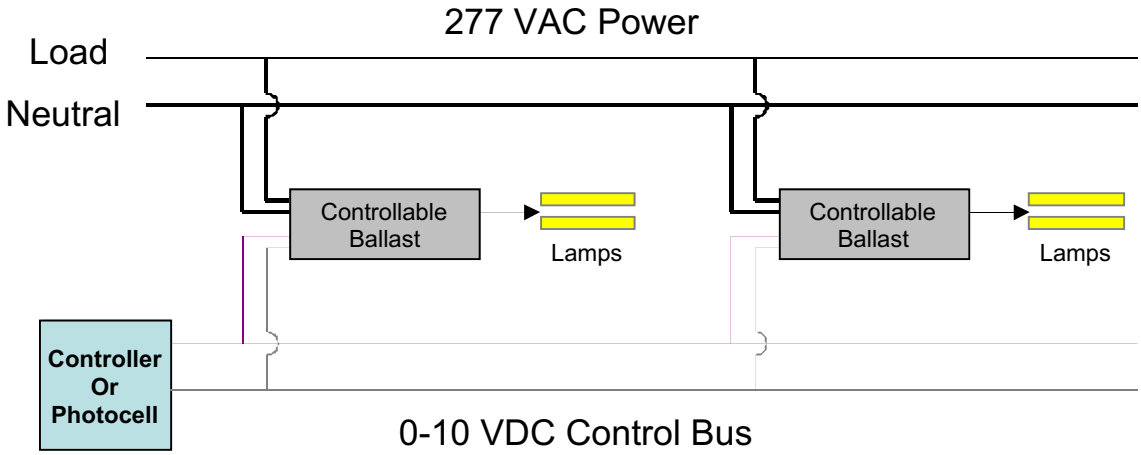


Figure 1. Wiring diagram for the low-voltage control circuit used in most commercially available 0-10 VDC controllable fluorescent lamp ballasts.

Designing the First Interface

Our initial task was to design a proof-of-concept interface that would allow control of the 0-10 VDC controllable ballast from a digital LAN. Pete Pettler researched the market in 1999 and identified Dallas Semiconductor as the manufacturer with the hardware (microchips) and the communications LAN (1-wire LAN) that was most appropriate to our purpose.

Pettler designed the ballast network interface around the microchip set from Dallas Semiconductor. The initial circuit design proof-of-concept was as shown in **Figure 2** below.

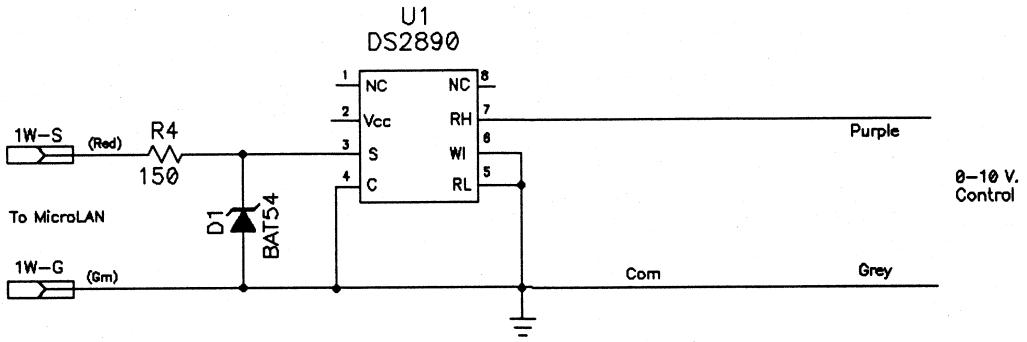


Figure 2. Circuit diagram for first proof-of-concept for the IBECS network/ballast interface.

The above circuit contains the Dallas Semiconductor DS 2890 digital potentiometer along with the other circuitry required to serve as the network interface for any 0-10 VDC controllable fluorescent ballast that can source current (most commercially available controllable ballasts are able to do this). Consequently, the network interface above requires no additional power. The power to drive the communications portion of the digital pot is borrowed from the MicroLan itself. The current to drive the dimming portion is provided by the current sourced by the low-voltage leads from the controllable ballast.

The technical specifications for the Dallas Semiconductor digital potentiometer can be found at http://pdfserv.maxim-ic.com/arpdf/DS2890.pdf and in Appendix A to this report. Note the selection of this company's hardware to construct the interface does not imply that there are not other companies that have similar products and capabilities.

We packaged the above circuit in plastic as shown below (**Figure 3**). The two solid copper leads connect to the purple and grey wires from the controllable ballast. The pigtail wires connect to the microLAN. Once the microLAN is installed (using CAT5 cable or equivalent) each ballast to be controlled would be wired to an interface and the interface wired to the microLAN.

Figure 3. Image of the first IBECS network/ballast interface for communicating digitally with controllable fluorescent ballasts. The blue and white wires coming out of the top of the interface are connected to the purple and grey leads on a controllable ballast. The blue and white pigtails go to the digital microLAN.

Demonstration of Proof-of-Concept Prototype at LBNL Office

To test the above network interface, we installed six of the interfaces to control the overheads lights in an office at LBNL's Building 46 (**Figure 4**). The office consisted of four three-lamp luminaires that were tandem wired so that the in-board and out-board lamps could be separably switched using two manual wall switches (**Figure 5**). (Tandem wiring is code for non-residential California buildings under Title 24).

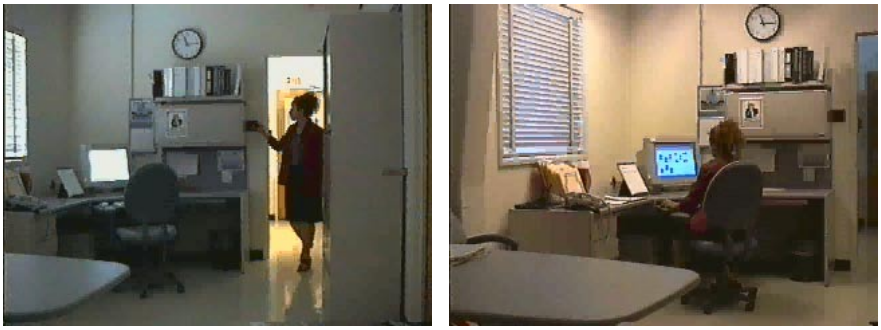


Figure 4. Images of office at LBNL Building 46 where the IBECS network interface was first tested. Left image shows a person entering the office and switching on the manual wall switches for the overhead lights. Right image shows the occupant working at the computer where the IBECS control software to control the overhead lights resides.

Figure 5. Images of the ceiling lights in office at LBNL Building 46 where the IBECS network interfaces were first tested. The upper left image shows the lights with both wall switches in the OFF position. The location of the installed low-voltage wire raceway is shown in the callout. The upper right image shows the lights with the in-board switch ON and the outboard switch OFF. The lower left image shows the lights with the outboard switch ON and the inboard switch OFF. The lower right image shows the lights with both switches in the ON position.

To test the IBECS network/ballast interfaces, the existing six, two-lamp, non-dimming, ballasts were replaced with 0-10 VDC two-lamp controllable ballasts from General Electric (GE B232SR120VS, product code 80355, 5-100% dimming). Each of the six installed dimming ballasts were equipped with a ballast network interface so they could be individually controlled. In addition, the electricians installed a low-voltage CAT-5 cable wire in a surface-mounted raceway connecting all the ballast interfaces (see **Figure 5**). We intended to run the IBECS microLAN on the CAT-5 cable. We terminated one end of the

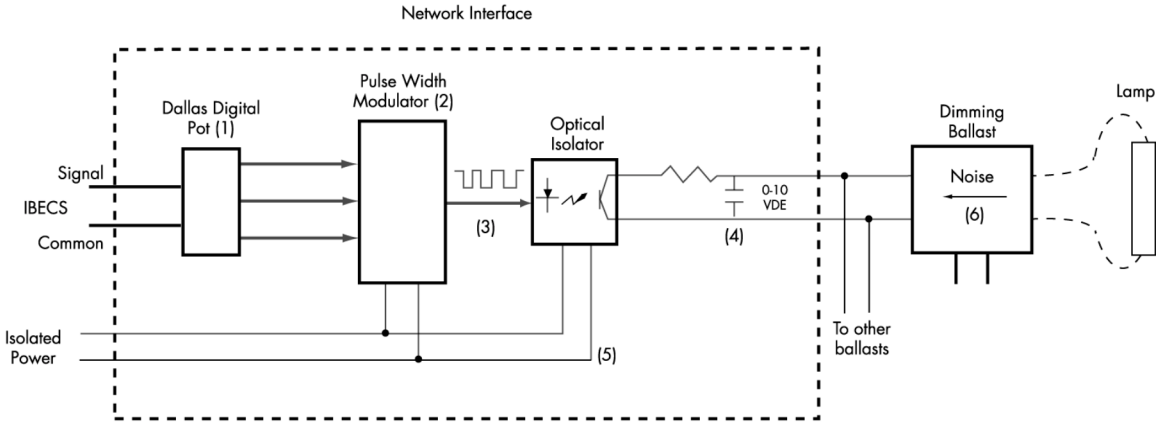
microLAN with an RS-232/microLAN bridge near the occupant's personal computer so that the occupant could dim the overhead lights to taste using IBECS. To complete the demonstration, we connected the bridge (HA3 adaptor from Point Six, http://www.pointsix.com) at the end of the run to the serial port on the PC where we installed the 1-wire control software from Advantech (GenieDAQ, http://www.advantech.com) and the DDE server (also from Point Six). [Note: the HA3 port adaptor has been superceded by subsequent port adaptor designs. Appendix A gives the port adaptor specifications for the Maxim DS9097E port adaptor, which is equivalent to the earlier HA3 adaptor]. We produced a simple control screen using the Advantech software that let us control 1-wire devices from the PC.

Our tests of the first interface were disappointing. Electronic noise generated by the ballast and injected back onto the low-voltage control circuit added a large noise signature onto the digital microLAN. Because each ballast is connected in parallel to the low-voltage circuit, the noise generated by each adds to the overall noise level. This noise swamped the signal level on the digital microLAN, this prevented the digital microLAN from communicating with the network interfaces. We did not detect this problem with our initial IBECS demonstration kit because that kit controlled only one interface and the wire runs were very short.

Once we identified the noise problem described above, we tested several other types of controllable ballasts and found that these ballasts also generated unacceptable electronic noise levels, although we found that the noise signature of different ballasts varied significantly. Our first solution was to add capacitors at the interface input terminals. However, this did not prove to be a reliable solution.

Development of the Refined Prototype

To solve the ballast noise interference problem identified above, Pettler made major modifications to the circuit shown in **Figure 1** in order to optically isolate the interface from noise interference generated by the controllable ballast. The circuit was entirely redesigned so that Dallas Semiconductor's digital potentiometer would control the ON-OFF ratio of a pulse width modulated (PWM) signal that is transmitted to the 0-10 volt input of the ballast(s) via an optical isolator as shown in **Figure 6** below.



(1) Dallas Semiconductor's V2890 digital potentiometer (6 pin)
(2) Single CMOS Integrated Circuit
(3) Fixed frequency output at approximately 200Hz with variable symmetry
(4) This single pole filter crudely converts pulse width modulation to 1-10V current sinking control
(5) Each dimming interface requires approximately 50 milliwatts of external power
(6) Any noise generated in the ballast cannot pass the optical isolator

Figure 6. Block diagram of the revised IBECS network/ballast interface designed to eliminate noise from the electronic ballast.

Since both the pulse width modulator and the optical isolator require external power (the digital pot does not), the above network interface requires a powered, i.e., four-wire IBECS network. Note that this is a departure from the initial prototype, which did not require any external power. Since the two obvious candidates for IBECS network cable (CAT 5 or standard Telco wiring) already contain at least four conductors, the cost per linear foot of network cable is only marginally more expensive with four wires than with two. The added robustness of the 4-wire system would more than make up for any marginal increases in wiring costs.

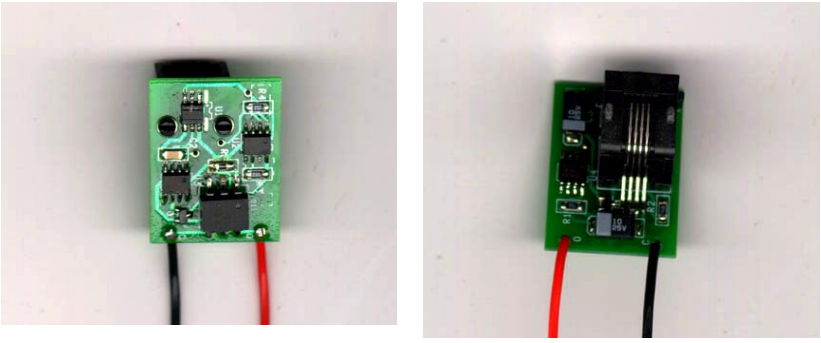


Figure 7. Bottom and top views of the final refined IBECS network/ballast interface. The red and black wires connect to the low-voltage "poke-thru" connector on the controllable ballast, while the IBECS microLAN plugs into the black RJ-11 connector on the top of the interface.

Network Considerations

Unlike the first prototype, the refined network interface cannot be self-powered. Several components on the circuit require external instrumentation power (clean 12 VDC) in order to operate correctly. This implies that the classic two-wire microLAN should be modified to consist of at least four wires (rather than just two) and that two of those wires must be dedicated to supplying low-voltage current to devices on the (modified) microLAN. These changes required that we re-think the network issues.

The refined ballast network prototypes use RJ-11 style modular jacks with telephone wire to form a "plug and play" control network. As shown in **Figure 8**, this allows additional ballast network interfaces to be "daisy-chained" together without the installer worrying about which of the inputs on the Y-splitter to use. This solution uses telephone cable that is wired in a particular way (called "network-wired" to distinguish it from the "telephone-style" wiring that is often used in homes.).

In **Figure 8** we have located the MicroLAN controller/bridge, which bridges between the microLAN and Ethernet, at one end of the microLAN run (although it can be located anywhere in the run). We have also shown a power supply at the other end of the microLAN run which will provide 12 VDC power to two wires of the telephone cable.

The above network wiring arrangement forms the basis of a reliable "plug-and-play" network that can be easily installed using existing telecommunications trade techniques.

Demonstrated Performance of the Refined Prototype

We modified the test office by replacing the old interfaces with the redesigned IBECS network/ballast interfaces to ascertain whether we had successfully treated the noise problem. We also added instrumentation voltage to the low-voltage cable using a simple DC power supply (called, curiously, a "wall wart").

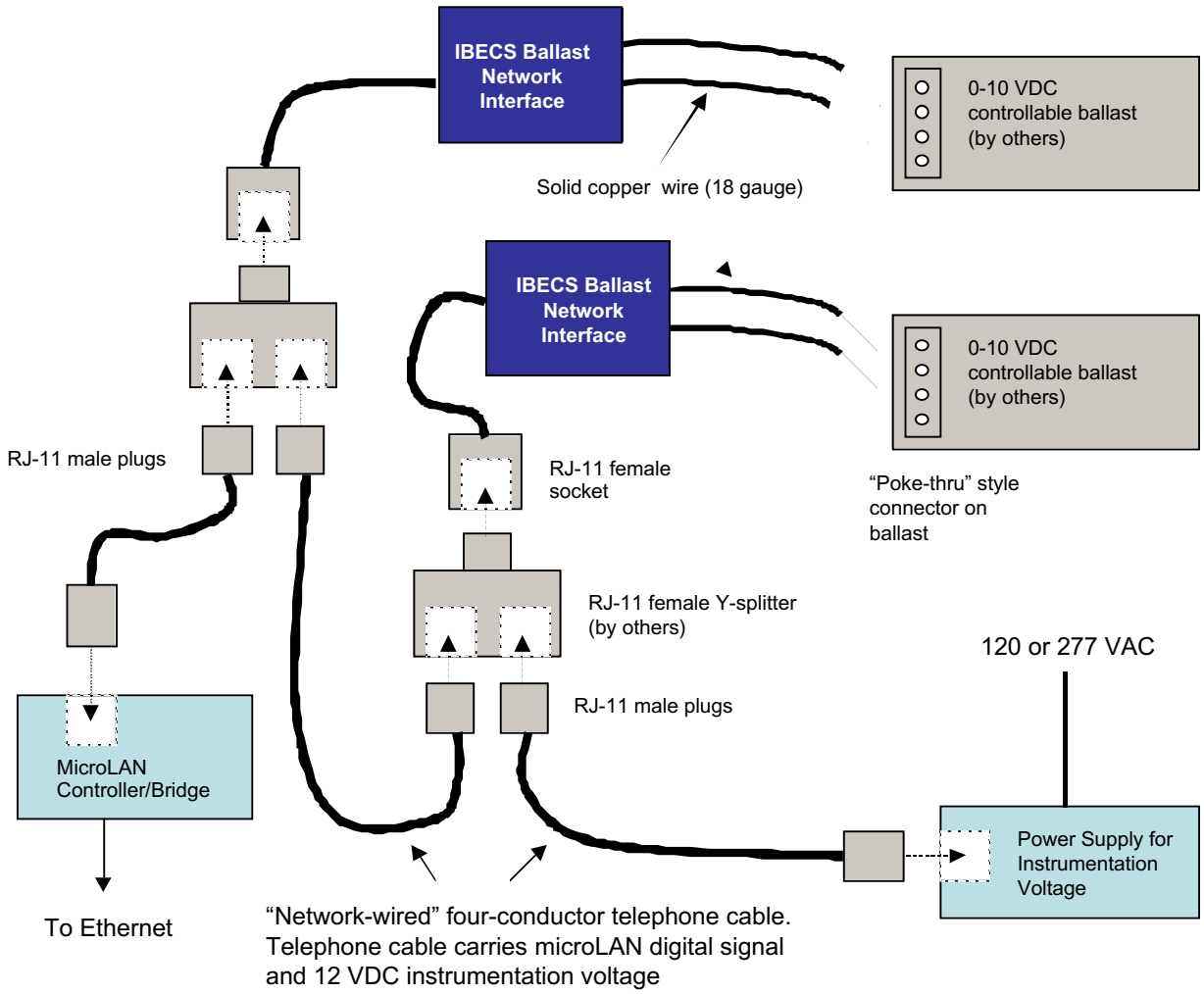


Figure 8. Diagram showing how the IBECS network/ballast interfaces would be daisy-chained together using a system of RJ-11 connectors and four-conductor telephone cable to form a robust "plug-and-play" network.

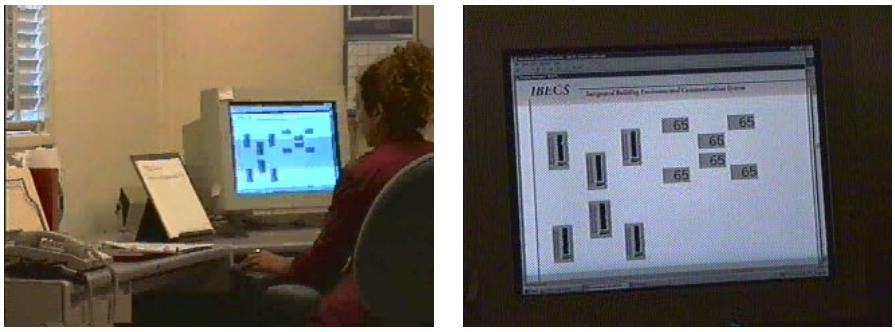


Figure 9. Left image shows occupant using IBECS to change the dim levels of the overhead lights using the computer. The right image is a closeup of the IBECS control screen. Note the six "sliders" on the left portion of the image each corresponding to a separately controlled ballast.

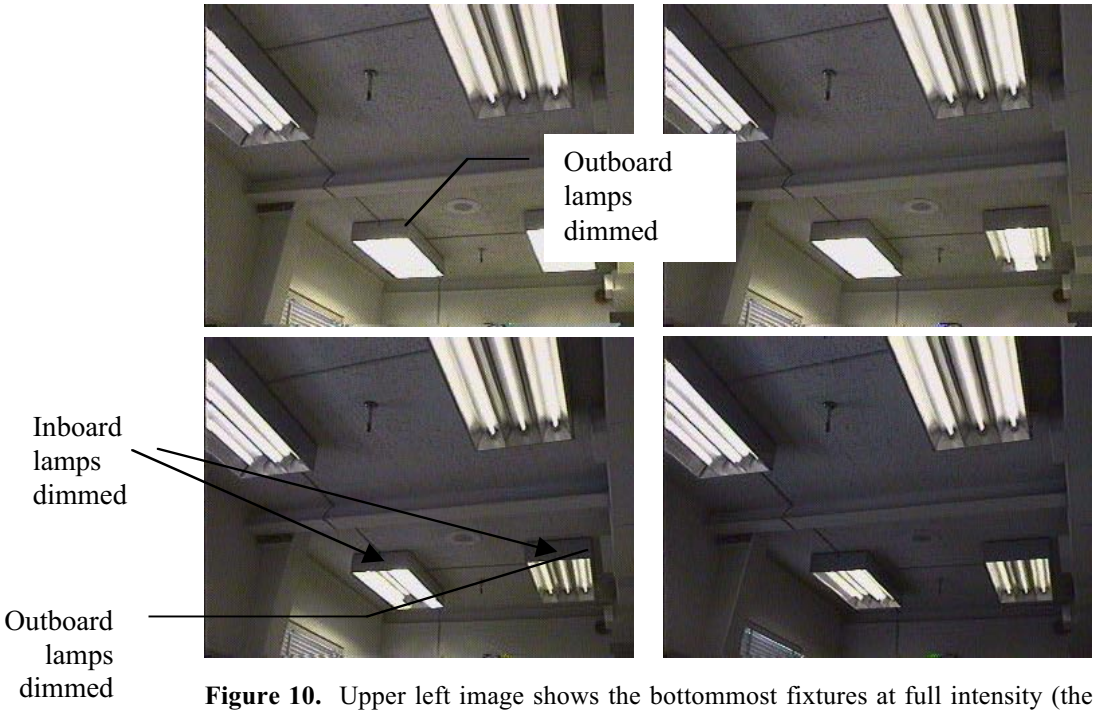


Figure 10. Upper left image shows the bottommost fixtures at full intensity (the topmost fixtures were set to low intensity in all images). Callouts indicate the dim state of the lights in the other two images. The lower right image shows all ballasts operating in fully dimmed state.

We found that the refined IBECS network/ballast interfaces worked very reliably in our test office. Not only could we control each ballast exactly as desired, but the lights dimmed very quickly without any discernable delay. All of the noise problems encountered with the first design have been eliminated. The refined interface eliminates noise from the following ballast types: Motorola Helios, GE, and Advance Mark VII). Although we have not tested this installation on other types of controllable ballasts, we are confident that the optical isolation techniques that we have employed should work for most 0-10 VDC controllable ballasts on the market today.

One practical aspect of this demonstration needs further comment. The 5-100% dimming ballasts that we used could be dimmed past the point of reliable operation by supplying a very small voltage from the interface (about 2 volts). We found that at this low dim level, the lamps would blacken and fail rapidly since the ballast was unable to maintain sufficient cathode voltage at the lowest setting. Fortunately, this problem was easy to fix in the controlling software. Simply by limiting the dimming level to a more modest voltage (easily done in software), we could use the IBECS control software to prevent the ballast from operating in a range where good performance could not be guaranteed. This is another advantage to the IBECS approach. Even if the light equipment is physically capable of operating the lamps at too low a light level, the IBECS control software can be tweaked easily by the installer to prevent the lamps from dimming too low. Needless to say, this is much cheaper to change in software than in the ballast control circuitry.

Conclusion

We learned that newly available silicon microchips are a suitable platform for designing low-cost digital network/ballast interfaces that are useful for enabling network operation of commercially available dimming ballasts. We found that electrical noise generated by the ballast in the 0-10 VDC controllable loop can interfere with digital network operation unless the interface is hardened from this noise. Using optical isolation, we produced a refined IBECS network/ballast interface that can provide universal control of most available 0-10 VDC controllable ballasts. In quantities, we estimate that the cost of the

universal IBECS network/ballast interface would be about $1 to $2 to OEMs. This is 5 to 10 times cheaper per unit than any other proposed communications system that we are familiar with.

Thus we successfully completed the task objectives by designing, developing, fabricating and demonstrating an IBECS network/ballast interface that is useful for economically dimming controllable ballasts.

Acknowledgement

This work was supported by the Assistant Secretary for Energy Efficiency and Renewable Energy, Office of Building Technology, State and Community Programs, Office of Building Research and Standards of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

APPENDIX A: Parts Specifications

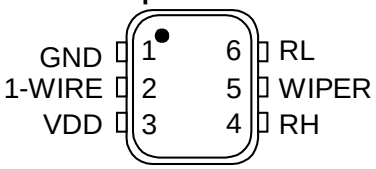
DS2890
1-Wire® Digital Potentiometer

FEATURES

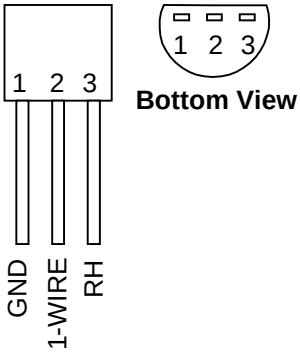
- Single element 256-position linear taper potentiometer
- Supports potentiometer terminal working voltages up to 11V
- Potentiometer terminal voltage independent of supply voltage
- Potentiometer wiper position controlled and read over minimal 1-Wire bus interface
- 100 kΩ resistor element value
- Provides 1-Wire and V_{DD} power modes
- Supports Conditional Search based on power-on default wiper position
- Multiple DS2890's can be identified on a common 1-Wire bus and operated independently
- Unique factory lasered 64-bit registration number assures error free device selection and absolute part identity
- Built-in multi-drop controller ensures compatibility with other 1-Wire Network products
- Supports Overdrive mode which boosts communication speed up to 142 kbits per second
- -40°C to +85°C operating temperature range
- 2.8V – 6.0V operating voltage range

PIN ASSIGNMENT

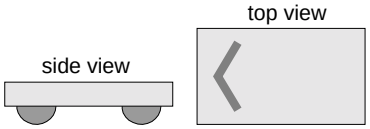
Top View
6-pin TSOC



TO-92 Package



Flip Chip Package



Visit www.dalsemi.com for Flip Chip pinout and mechanical data.

ORDERING INFORMATION

PART NUMBER	RESISTANCE*	PACKAGE DESCRIPTION
DS2890-000	100 kΩ	T0-92
DS2890P-000	100 kΩ	6-pin TSOC
DS2890X-000	100 kΩ	Flip Chip Pkg., Tape & Reel
DS2890T-000	100 kΩ	Tape & Reel of DS2890
DS2890V-000	100 kΩ	Tape & Reel of DS2890P

* Contact the factory for availability of alternate resistance values

PIN DESCRIPTION

SIGNAL NAME	TYPE	FUNCTION
1-WIRE	I/O	1-Wire bus interface. Open drain, requires external pull-up resistor. Range: 2.8V – 6.0V. See HARDWARE CONFIGURATION for pull-up resistor recommendations.
RH	I/O	High end terminal of potentiometer resistor element. Range: 0V – 11.0V. Range independent of 1-Wire or V_{DD} supply levels as well as the voltage levels applied to the other potentiometer terminals.
RL	I/O	Low end terminal of potentiometer resistor element. Range: 0V – 11.0V. Range independent of 1-Wire or V_{DD} supply levels as well as the voltage levels applied to the other potentiometer terminals.
WIPER	I/O	Potentiometer wiper terminal. Range 0V – 11.0V. Range independent of 1-Wire or V_{DD} supply levels as well as the voltage levels applied to the other potentiometer terminals.
V_{DD}	PWR	Auxiliary power supply input. Range: 2.8V – 6.0V
GND	PWR	Ground

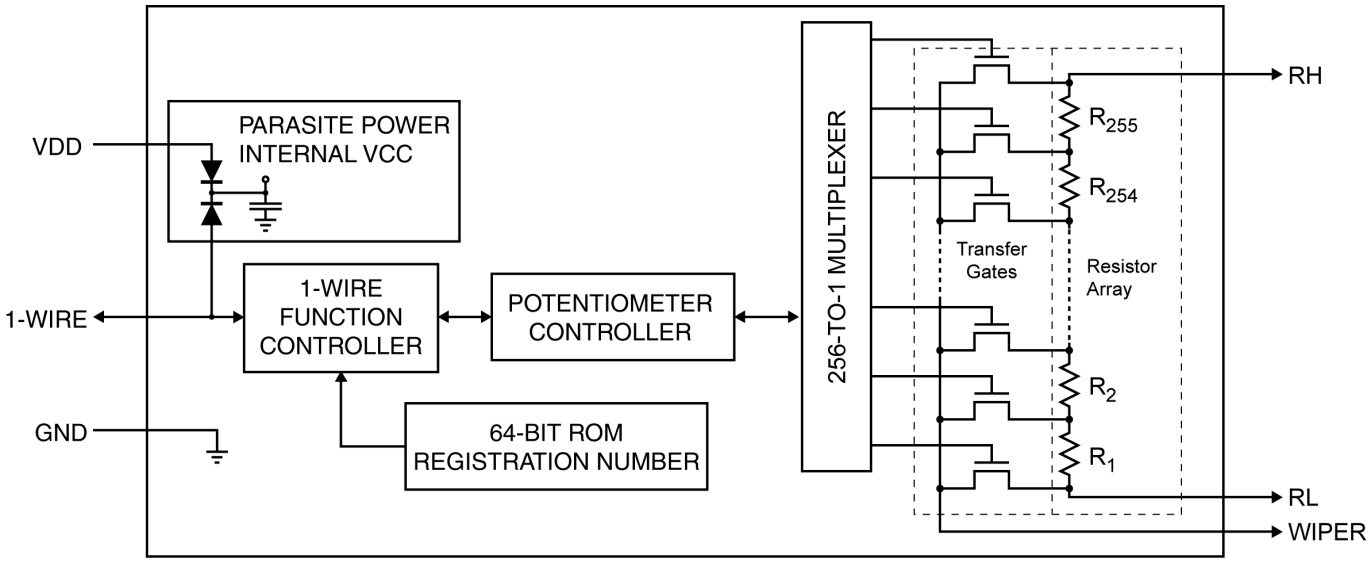
DESCRIPTION

The DS2890 is a linear taper digitally controlled potentiometer with 256 wiper positions. Device operation, including wiper position, is controlled over the single contact 1-Wire bus for the ultimate in electrical interface simplicity. With a wide 0–11 volt working voltage range for the potentiometer terminals, the DS2890 is ideal for a broad range of industrial and control applications. Potentiometer terminal voltage is independent of device supply voltage as well as the voltage applied to the other potentiometer terminals. Communication with the DS2890 follows the standard Dallas Semiconductor 1-Wire protocol and can be accomplished with minimal hardware such as a single port pin of a microcontroller. Multiple DS2890 devices can reside on a common 1-Wire bus and be operated independently of each other. Each DS2890 has its own unalterable 64-bit ROM registration number that is factory lasered into the chip. The registration number guarantees unique identification for absolute traceability and is used to address the device in a multi-drop 1-Wire Network environment. The DS2890 will respond to a 1-Wire Conditional Search command if the potentiometer wiper is set at the power-on default position. This feature enables the bus master to easily determine whether a potentiometer has gone through a power-on reset and needs to be re-configured with a required wiper position setting. The DS2890 supports two power modes: 1-Wire only mode in which device power is supplied parasitically from the 1-Wire bus or V_{DD} mode where power is supplied from an external supply; when operating from V_{DD} mode wiper resistance is reduced.

OPERATION

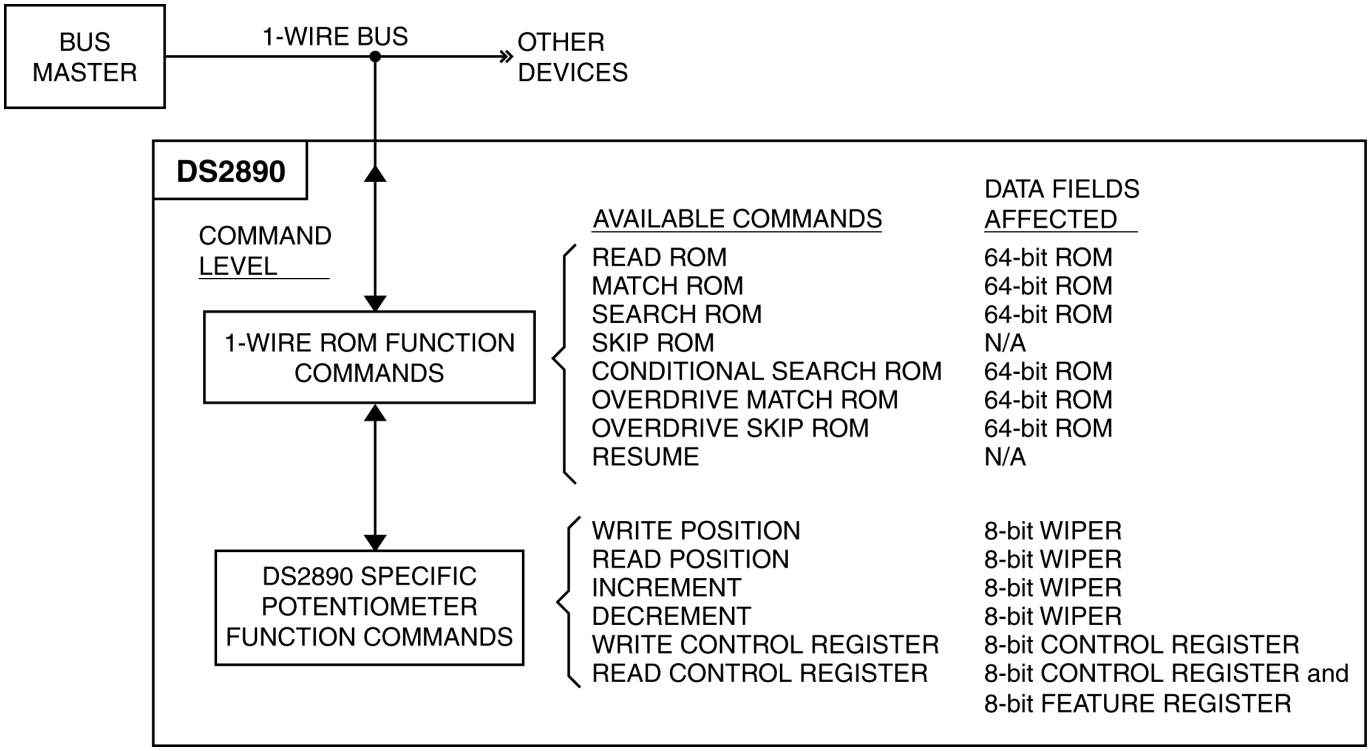
The DS2890 is a single element digital potentiometer; a block diagram of the device is shown in Figure 1. The device has a total of 256 linearly spaced tap points including the RL and RH terminals; a total of 255 resistive segments exist between the RL and RH terminals. These tap points are accessible to the WIPER terminal whose position is controlled via the 1-Wire bus interface. Wiper position and device state are maintained as long as the 1-Wire bus is active or the V_{DD} supply is applied within operating limits. Otherwise, a power-on reset will occur and the wiper position and operating state will return to power-on default conditions.

Figure 1. **DS2890 BLOCK DIAGRAM**



As shown in the figure the device has five major elements: the 1-Wire Function Controller, the Potentiometer Controller, the 64-bit ROM, the resistor array, and Parasite Power circuitry. Each of these elements is discussed in detail throughout the remainder of the data sheet. DS2890 control including device selection, positioning/reading the potentiometer wiper, and device operating state is performed over the 1-Wire bus. The hierarchical structure of the 1-Wire protocol as applicable to the DS2890 is shown in Figure 2. As shown, the control sequence starts with the 1-Wire bus master issuing one of eight ROM function commands. After a ROM function command is successfully completed potentiometer functions may be executed. The protocol for ROM and potentiometer functions are described in the "COMMAND FLOW" section**.** For the 3-pin TO-92 package configuration and operation see the "TO-92 PACKAGE OPERATION" section.

Figure 2. **1-WIRE COMMAND HIERARCHICAL STRUCTURE**



DATA I/O BIT ORDER

All data is read and written least significant bit (LSB) first.

POTENTIOMETER FEATURE REGISTER

Although the feature set of the DS2890 is primarily fixed, a mechanism to identify feature characteristics of future 1-Wire potentiometers has been developed and implemented in the DS2890. As shown in Figure 3, the feature register is an encoded read-only byte that describes the characteristics of the DS2890 and future 1-Wire potentiometers. Feature values that correspond to the DS2890 are highlighted. The feature register is read with the READ CONTROL REGISTER potentiometer function command (see “POTENTIOMETER FUNCTION COMMANDS”).

Figure 3. **1-WIRE POTENTIOMETER FEATURE REGISTER**

Feature Register Bit Encoding

b7	b6	b5	b4	b3	b2	b1	b0
PR		NWP		NP		WSV	PC

Feature Register Bit Definitions

Feature Description	Bit(s)	Definition
PC: potentiometer characteristic	b0	If 0: logarithmic potentiometer element(s) If 1: linear potentiometer element(s)
WSV: wiper setting volatility	b1	If 0: wiper setting(s) are non-volatile If 1: wiper setting(s) are volatile
NP: number of potentiometers	b3..b2	2 bit binary value representing number of potentiometers: If 00b: 1 potentiometer If 01b: 2 potentiometers If 10b: 3 potentiometers If 11b: 4 potentiometers
NWP: number of wiper positions	b5..b4	2 bit binary value representing number of wiper positions for each potentiometer: If 00b: 32 positions If 01b: 64 positions If 10b: 128 positions If 11b: 256 positions
PR: potentiometer resistance	b7..b6	2 bit binary value representing potentiometer resistance: If 00b: 5 kΩ If 01b: 10 kΩ If 10b: 50 kΩ If 11b: 100 kΩ

DS2890 feature values are highlighted: value

The DS2890 will respond with a feature register value of F3h when a READ CONTROL REGISTER command is executed, see section "POTENTIOMETER FUNCTION COMMANDS".

POTENTIOMETER CONTROL REGISTER

The potentiometer control register is used to turn on/off the DS2890 charge pump (see section "POTENTIOMETER WIPER RESISTANCE AND CHARGE PUMP CONSIDERATIONS" for a discussion of the charge pump) and has control capabilities for future 1-Wire potentiometers that could contain multiple resistor elements. The format of the control register is shown in Figure 4.

Figure 4. **POTENTIOMETER CONTROL REGISTER**

Control Register Bit Encoding

b7	b6	b5	b4	b3	b2	b1	b0
X	CPC	X	X	$\overline{WN}$		WN	

Control Register Bit Definitions*

Description	Bit(s)	Definition
WN: wiper number to control	b1..b0	2 bit binary value representing the potentiometer wiper to control:
		If 00b: potentiometer 1 wiper
		If 01b: potentiometer 2 wiper
		If 10b: potentiometer 3 wiper
		If 11b: potentiometer 4 wiper
$\overline{WN}$: inverted wiper number to control	b3..b2	1's complement of potentiometer wiper to control:
		If 11b: potentiometer 1 wiper
		If 10b: potentiometer 2 wiper
		If 01b: potentiometer 3 wiper
		If 00b: potentiometer 4 wiper
CPC: charge pump control	b6	If 0: the charge pump is OFF If 1: the charge pump is ON
X: don't care.	b4,b5,b7	These bits are reserved for future use by Dallas Semiconductor. These bits should be written to a value of 0.

*NOTE:

Control Register power-on defaults: Charge Pump is OFF (CPC=0), Wiper Number to control is wiper #1 (WN=00b, $\overline{\mathbf{WN}}$=11b).

Valid DS2890 control values are highlighted: value
Thus for the DS2890, valid control register values are:

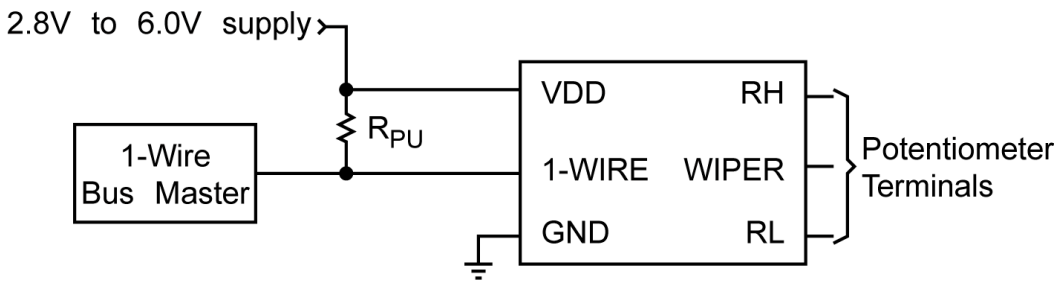
Control Register Value	Description
00001100b	charge pump off, potentiometer #1 wiper selected
01001100b	charge pump on, potentiometer #1 wiper selected

As shown in Figure 17 and discussed in the "POTENTIOMETER FUNCTION COMMANDS" section, no change in device state will occur if an invalid control register value is sent.

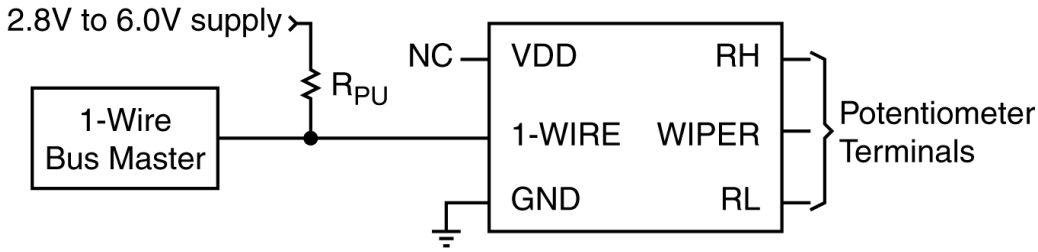
POWER

With the charge pump off, the DS2890 can derive its power entirely from the 1-Wire bus by storing energy on an internal capacitor during periods of time when the 1-Wire bus is in a high state. During bus low times the device continues to operate from the energy stored on the internal capacitor; the capacitor is then recharged when the bus returns to a high state. This technique of operating entirely from the 1-Wire bus by powering from energy stored on an internal capacitor during bus low times in known as "parasite powered" operation. As an option, an auxiliary power source may be connected to the V_{DD} power pin. The auxiliary power mode is appropriate for applications where device charge pump activation is necessary, the device may be temporarily disconnected from the 1-Wire bus, or bus low times may be very long. See Figure 5 for example configurations for both power modes.

Figure 5. **POWER SUPPLY CONFIGURATION OPTIONS**



(a) Auxiliary V_{DD} Supply Configuration



(b) 1-Wire Parasite Power Configuration

POTENTIOMETER WIPER RESISTANCE AND CHARGE PUMP CONSIDERATIONS

A simplified diagram of the DS2890 resistor array is shown in Figure 6. In this figure the r_{DS} resistance of the wiper transistors in Figure 1 are modeled as wiper resistance R_{WIPER}. The value of R_{WIPER} varies with device configuration, operational state, and wiper terminal voltage. If an auxiliary external V_{DD} supply configuration is used as shown In Figure 5a, the DS2890 charge pump may be enabled to reduce potentiometer wiper resistance. A consequence of enabling the charge pump is increased device power consumption. This increase is beyond the level that can be supported when operating in 1-Wire parasite power mode (see POWER section). Therefore if it is necessary to enable the charge pump in an application, the power supply configuration as shown in Figure 5a **must** be used. Figure 7 and Figure 8 are graphs of wiper resistance with the charge pump turned ON and OFF respectively.

Figure 6. **POTENTIOMETER RESISTOR MODEL**

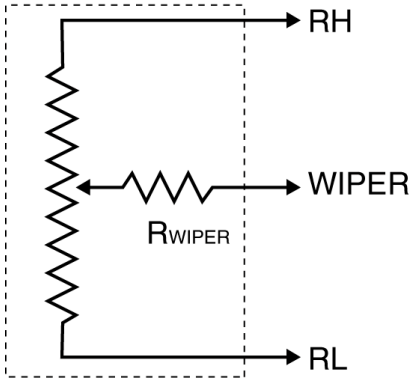


Figure 7. **TYPICAL WIPER RESISTANCE VS WIPER VOLTAGE, CHARGE PUMP ON**

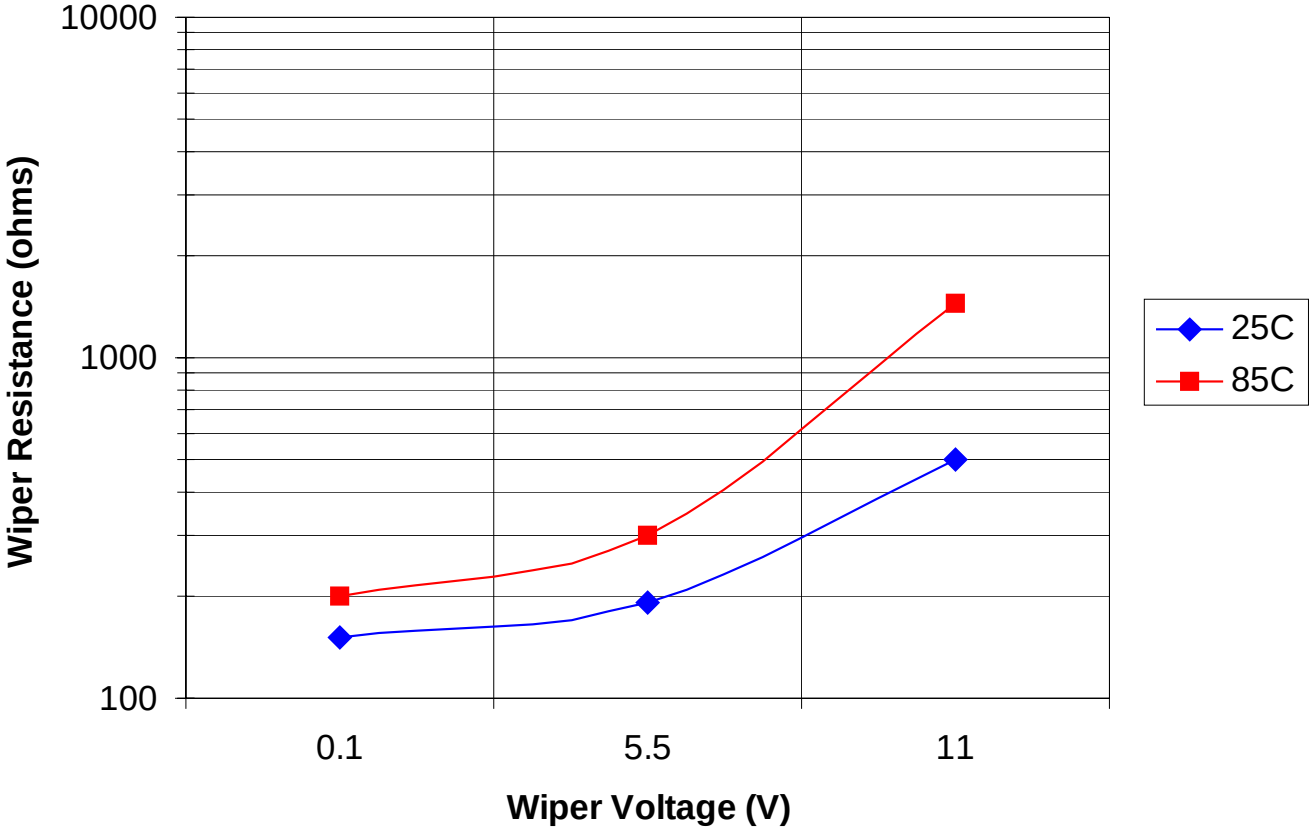
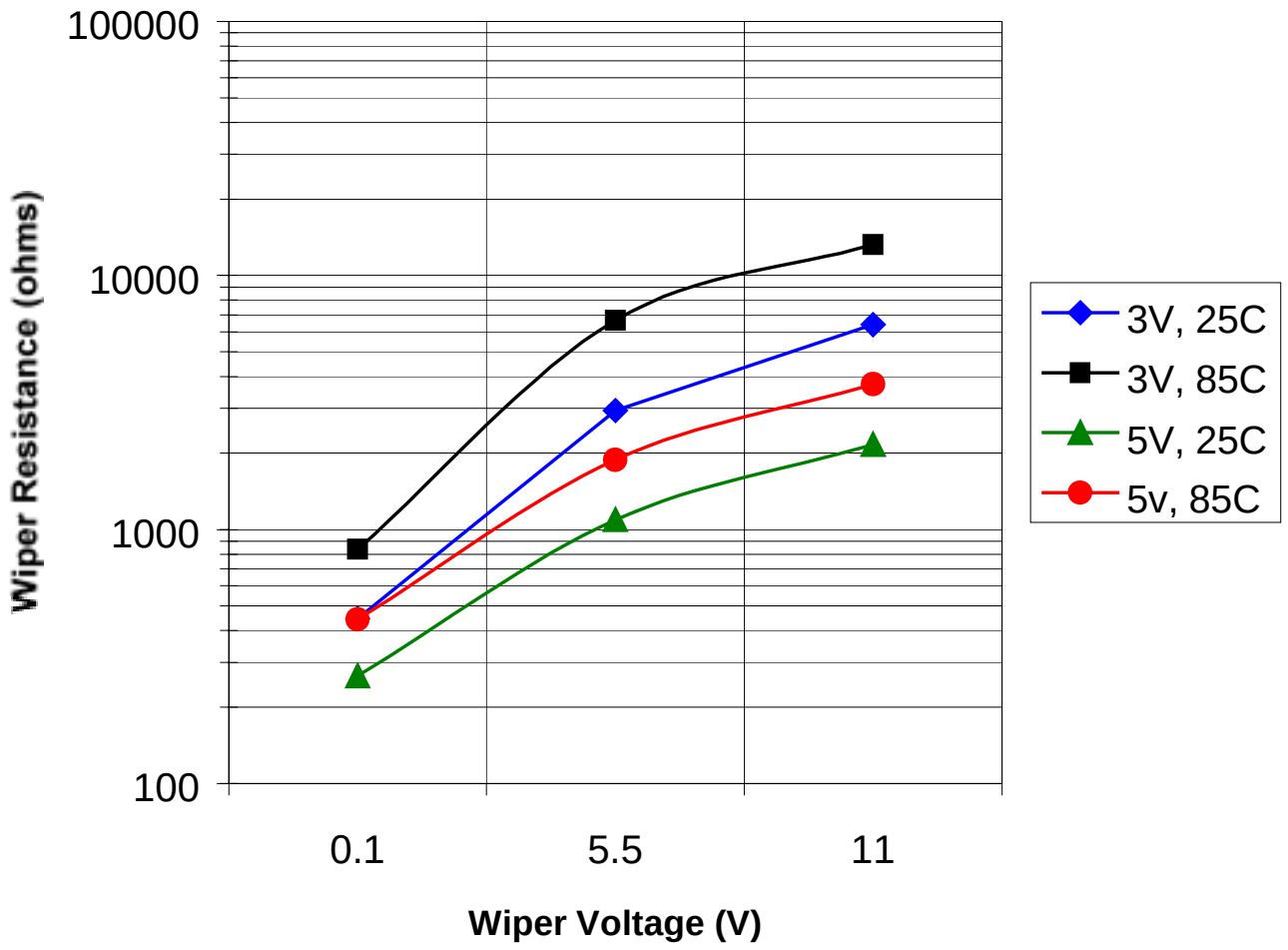


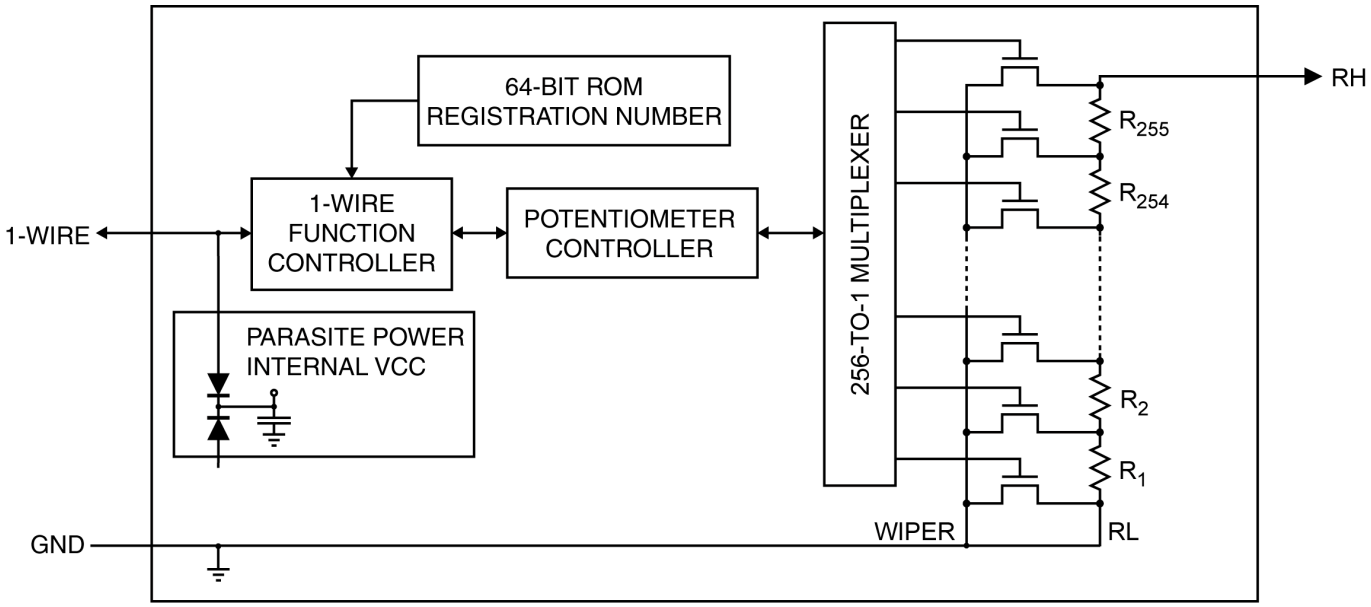
Figure 8. **TYPICAL WIPER RESISTANCE VS WIPER VOLTAGE, CHARGE PUMP OFF**



TO-92 PACKAGE OPERATION

When packaged in a 3-pin TO-92, the DS2890 takes on a configuration as shown in Figure 9. As shown, the RL and Wiper terminals and are connected to GND and the resistance between the RH terminal and GND is varied. Note that the DS2890 charge pump must be turned off (default state) for this configuration. (This is a power consumption issue as described in the section "POTENTIOMETER WIPER RESISTANCE AND CHARGE PUMP CONSIDERATIONS".)

Figure 9. **DS2890 TO-92 CONFIGURATION BLOCK DIAGRAM**



64-BIT LASTERED ROM

Each DS2890 contains a unique ROM registration number that is 64 bits long; the format of this value is shown in Figure 10. The first 8 bits are a 1-Wire family code; the family code for the DS2890 and future 1-Wire Potentiometers is 2Ch.. The next 48 bits are a unique serial number that is administered by Dallas Semiconductor. The last 8 bits are a CRC of the first 56 bits. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 11. Operationally, the CRC generator works as follows: The shift register bits are first initialized to zero. Then starting with the least significant bit, the 8-bit family code is shifted in. After the 8th bit of the family code has been entered, the 48-bit serial number is shifted in. After shifting in the 48th bit of the serial number the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to an all zeros value. Detailed information about the Dallas 1-Wire Cyclic Redundancy Check is available in the Book of DS19xx iButton Standards. The 64-bit ROM and the 1-Wire Function Controller portions of the DS2890 allow the device to operate as a 1-Wire device and follow the protocol detailed in the section "TRANSACTION SEQUENCE".

Figure 10. **64-BIT LASERED ROM**

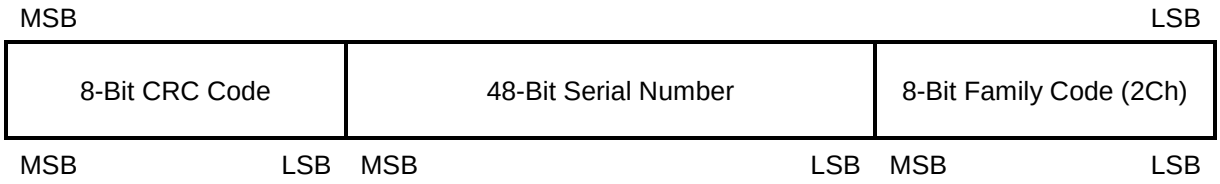
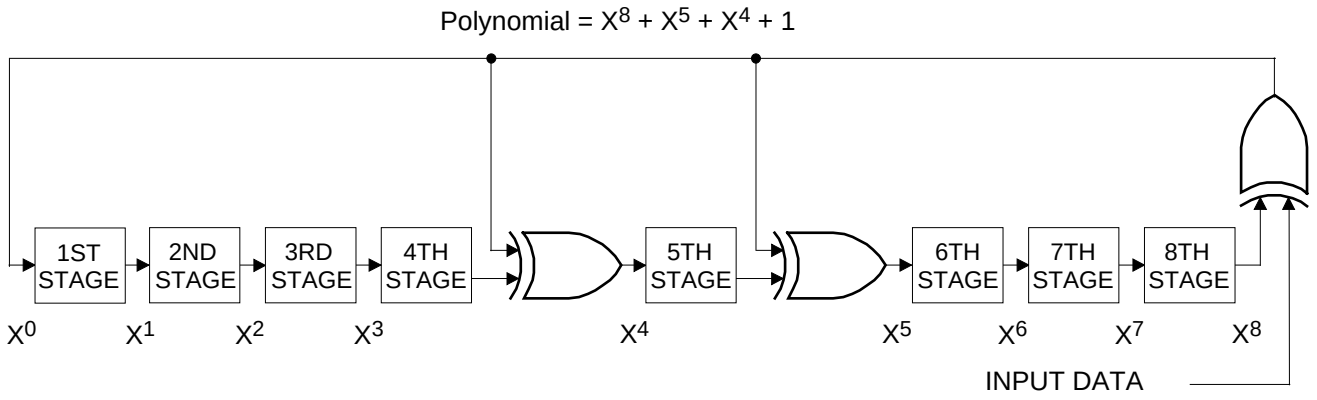


Figure 11. **1-WIRE CRC GENERATOR**



POTENTIOMETER FUNCTION COMMANDS

Once the bus master has completed a ROM command sequence, one of six DS2890 potentiometer function commands can be issued. The Potentiometer Function Command flow charts, Figure 16 and Figure 17, describe the protocols necessary for adjusting or reading the potentiometer wiper position or controlling the operating state of the DS2890. All potentiometer functions consist of a single command byte followed by one or more bytes of data or control written/read by the bus master. All data transferred between the DS2890 and the bus master are communicated least significant bit first.

READ POSITION [F0H]

The Read Position command is used to obtain the wiper setting of the potentiometer currently addressed by the Control Register. Although the DS2890 is a single element potentiometer, wiper addressing still applies and the Control Register wiper number used for addressing must be set accordingly. In addition to wiper position, the Control Register byte will be returned with a Read Position command. This enables the bus master to easily confirm/determine the currently addressed potentiometer wiper. Following the Read Position command byte, the bus master reads 16 bits to obtain first the Control Register byte then the wiper position byte. The DS2890 will respond with 0's to additional reads after the 8 bit of the position byte. The Read Position command is terminated with a Reset pulse.

WRITE POSITION [0FH]

The Write Position command is used to set the position of the currently addressed potentiometer wiper. Although the DS2890 is a single element potentiometer, wiper addressing still applies and the Control Register wiper number used for addressing must be set accordingly. The bus master follows the Write Position command byte with an 8-bit wiper position value. Following the 8th bit of the position byte, the bus master reads back the 8-bit position value from the DS2890 to confirm that the value was received correctly by the device. If an incorrect value is read back, the bus master must issue a Reset pulse and repeat the sequence. If the value read back is correct, the bus master then sends the 8-bit release code (96h). If the DS2890 accurately receives the release code, the wiper position is updated and the device will respond with 0's to additional reads by the bus master. If an invalid release code is received, no change is made to the wiper position and the device will respond with 1's to additional reads by the bus master. The Write Position command is terminated with a Reset pulse.

READ CONTROL REGISTER [AAH]

The Read Control Register command is used to obtain both the Control Register and potentiometer Feature Register. Following the Read Control Register command byte, the bus master reads 16 bits to obtain first the Feature Register byte and then the Control Register byte. The DS2890 will respond with 0's to additional reads after the 8 bit of the Control Register byte. The Read Control Register command is terminated with a Reset pulse.

WRITE CONTROL REGISTER [55H]

The Write Control Register command is used to manipulate DS2890 state bits located in the Control Register. This command is used to set the potentiometer wiper address and charge pump state. The bus master follows the Write Control Register command byte with an 8-bit register value. Following the 8th bit of the register byte, the bus master reads back the 8-bit control value from the DS2890 to confirm that the device received the correct value (Note that if an invalid register value was received by the DS2890, the bus master will read all 1's (FFh) during the read back sequence.). If a value other than FFh is read, the bus master determines if the DS2890 received the correct value. If an incorrect value is read back, the bus master must issue a Reset pulse and repeat the sequence. If the value read back is correct, the bus master then sends the 8-bit release code (96h). If the DS2890 accurately receives the release code, the Control Register is updated and the device will respond with 0's to additional reads by the bus master. If an invalid release code is received, no change is made to the Control Register and the device will respond with 1's to additional reads by the bus master. The Write Control Register command is terminated with a Reset pulse.

INCREMENT [C3H]

The Increment command is used for a one step position increase of the currently addressed potentiometer wiper. Although the DS2890 is a single element potentiometer, wiper addressing still applies and the Control Register wiper number used for addressing must be set accordingly. The bus master follows the Increment command byte with an 8-bit read to which the DS2890 will respond with the new 8-bit wiper position set point. No position change is made if the DS2890 wiper is at the maximum position (FFh) and an Increment command is received. One difference between the Increment/Decrement commands and other potentiometer functions is that upon completion of either of these commands, 1-Wire command processing remains at the potentiometer function level. As shown in Figure 16, additional potentiometer commands may be sent without going through the ROM function flow.

DECREMENT [99H]

The Decrement command is used for a one step position decrease of the currently addressed potentiometer wiper. Although the DS2890 is a single element potentiometer, wiper addressing still applies and the Control Register wiper number used for addressing must be set accordingly. The bus master follows the Decrement command byte with an 8-bit read to which the DS2890 will respond with the new 8-bit wiper position set point. No position change is made if the DS2890 wiper is at the minimum position (00h) and a Decrement command is received. One difference between the Increment/Decrement commands and other potentiometer functions is that upon completion of either of these commands, 1-Wire command processing remains at the potentiometer function level. As shown in Figure 16, additional potentiometer commands may be sent without going through the ROM function flow.

1-WIRE BUS SYSTEM

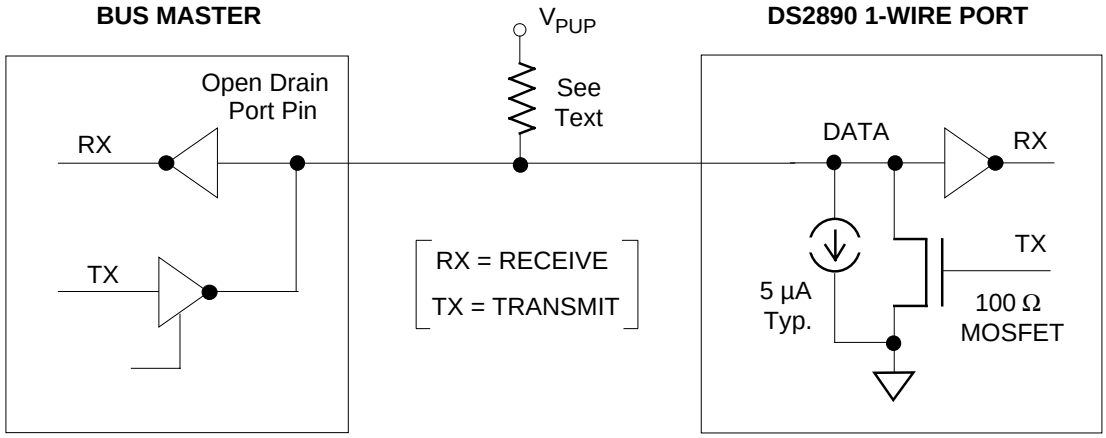
The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances the DS2890 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or 3-state outputs. The 1-Wire port of the DS2890 is open drain with an internal circuit equivalent to that shown in Figure 9. A multi-drop bus consists of a 1-Wire bus with multiple slaves attached. At regular speed the 1-Wire bus has a maximum data rate of 16.3 kbits per second. The speed can be boosted to 142 kbits per second by activating the Overdrive Mode. For a discrete bus master interface as in Figure 12, the 1-Wire bus requires a pull-up resistor with a minimum value of 2.2 kΩ. Depending on 1-Wire communication speed, regular or overdrive, and bus load characteristics, the optimal pull-up resistor value will be in the 1.5 kΩ to 5 kΩ range. Figure 13 shows a DS2480B bus master configuration with an interface to the host CPU serial port. Among many features, the DS2480B simplifies the 1-Wire interface design, generates slew-rate controlled 1-Wire waveforms, and off-loads 1-Wire timing generation overhead required in a discrete solution.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16 µs (Overdrive Speed) or more than 120 µs (regular speed), one or more devices on the bus may be reset.

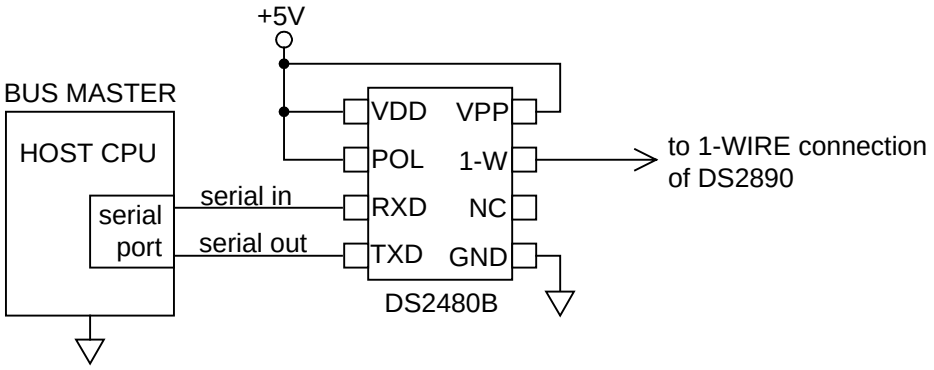
Figure 12. **HARDWARE CONFIGURATION**



NOTE:

Depending on 1-Wire communication speed, regular or overdrive, and bus load characteristics, the optimal pull-up resistor value will be in the 1.5 kΩ to 5 kΩ range.

Figure 13. **BUS MASTER WITH DS2480B DRIVER**



TRANSACTION SEQUENCE

The protocol for accessing the DS2890 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Potentiometer Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2890 is on the bus and is ready to operate. For more details, see the “1-WIRE SIGNALING” section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the eight ROM function commands that the DS2890 supports. All ROM function commands are 8 bits long. A list of these commands follows (refer to Figure 18 and Figure 19 flowcharts):

READ ROM [33H]

This command allows the bus master to read the DS2890’s 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number read by the master will be invalid.

MATCH ROM [55H]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2890 on a multi-drop bus. Only the DS2890 that exactly matches the 64-bit ROM sequence will respond to the following memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0H]

When a multi-drop system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the 64-bit ROM code of one device. Additional passes will identify the ROM codes of the remaining devices. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a search ROM, including an actual example.

CONDITIONAL SEARCH ROM [ECH]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified search condition will participate in the search. The device condition that will cause individual DS2890s to participate in a Conditional Search is a wiper position located at the power-on default setting (00h). This feature enables the bus master to easily determine whether a potentiometer has gone through a power-on reset and needs to be re-configured with a required wiper position setting.

SKIP ROM [CCH]

This command can save time in a single drop bus system by allowing the bus master to access potentiometer functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wired-AND result).

OVERDRIVE SKIP ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command the Overdrive Skip ROM sets the DS2890 in the Overdrive Mode. All communication following this command code has to occur at Overdrive Speed until a reset pulse of minimum 480 µs duration resets all devices on the bus to regular speed.

When issued on a multi-drop bus this command will set all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This will speed up the search process. If more than one Overdrive-supporting slave is present on the bus and the Overdrive Skip ROM command is followed by a read command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wire-AND result).

OVERDRIVE MATCH ROM [69H]

The Overdrive Match ROM command, followed by a 64-bit ROM sequence transmitted at Overdrive Speed, allows the bus master to address a specific DS2890 on a multi-drop bus and to simultaneously set it in Overdrive Mode. Only the DS2890 that exactly matches the 64-bit ROM sequence will respond to the subsequent potentiometer function command. Slaves already in Overdrive mode from a previous Overdrive Skip or a successful Overdrive Match command will remain in Overdrive mode. All Overdrive-capable slaves will return to regular speed at the next Reset Pulse of minimum 480 µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

RESUME COMMAND [A5H]

In a typical application the DS2890 may be accessed several times to complete a control adjustment. In a multi-drop environment this means that the 64-bit ROM sequence of a Match ROM command has to be repeated for every access. To maximize the data throughput in a multi-drop environment the Resume Command function was implemented. As shown in Figure 19, this function checks the status of the RC flag and, if it is set, directly transfers control to the potentiometer functions, similar to a Skip ROM command. The only way to set the RC flag is through successfully executing the Match ROM, Search ROM, Conditional Search ROM, or Overdrive Match ROM command. Once the RC flag is set, the device can repeatedly be accessed through the Resume Command function. Accessing another device on the bus will clear the RC flag, preventing two or more devices from simultaneously responding to the Resume Command function.

POTENTIOMETER FUNCTION EXAMPLE

At regular speed with an auxiliary supply (V_{DD} within range): turn on the charge pump, set the wiper position to mid-point, increment the wiper twice, and decrement the wiper once.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	Reset	Reset Pulse (480 - 960 µs)
RX	Presence	Presence Pulse
TX	CCh	Issue Skip ROM Command
TX	55h	Issue Write Control Register Command
TX	4Ch	Issue Control Register value for WN=0, CPC=1
RX	<data byte>	Read back Control Register value (4Ch) and verify
TX	96h	Issue Release Code to update Control Register
RX	<data bits>	If 0’s are read, update was successful; if 1’s are read, the update failed
TX	Reset	Reset Pulse (480 - 960 µs)
RX	Presence	Presence Pulse
TX	CCh	Issue Skip ROM Command
TX	0Fh	Issue Write Position Command
TX	7Fh	Write Wiper Position value
RX	<data byte>	Read back Wiper Position byte and verify
TX	96h	Issue Release Code to update Wiper Position
RX	<data bits>	If 0’s are read, update was successful; if 1’s are read, the update failed
TX	Reset	Reset Pulse
RX	Presence	Presence Pulse
TX	CCh	Issue Skip ROM Command

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	C3h	Issue Wiper Increment Command
RX	<data byte>	Read new wiper position
TX	C3h	Issue Wiper Increment Command
RX	<data byte>	Read new wiper position
TX	99h	Issue Wiper Decrement Command
RX	<data byte>	Read new wiper position
TX	Reset	Reset Pulse

1-WIRE SIGNALING

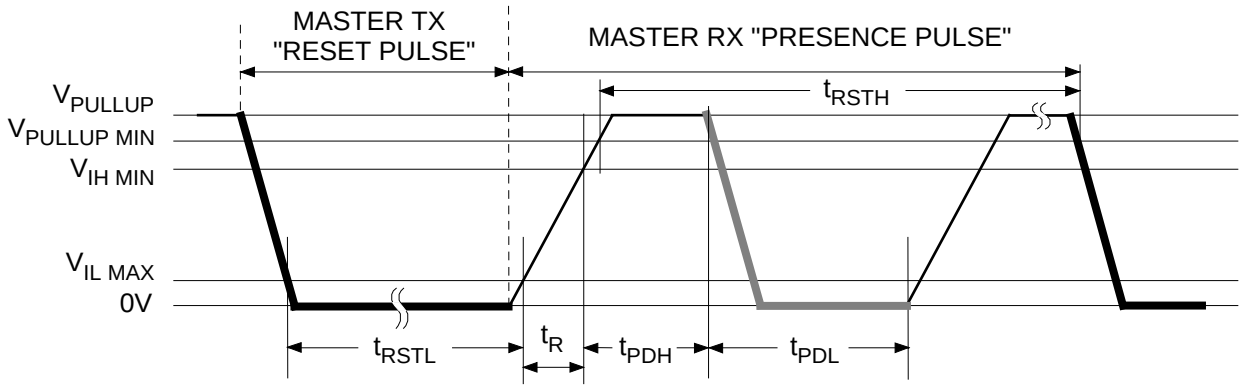
The DS2890 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1 and Read Data. Except for the presence pulse the bus master initiates all these signals. The DS2890 can communicate at two different speeds, regular speed and Overdrive Speed. If not explicitly set into the Overdrive mode, the DS2890 will communicate at regular speed. While in Overdrive Mode the fast timing applies to all waveforms.

The initialization sequence required to begin any communication with the DS2890 is shown in Figure 14. A Reset Pulse followed by a Presence Pulse indicates the DS2890 is ready to send or receive data. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480 µs at regular speed, 48 µs at Overdrive Speed). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pull-up resistor. After detecting the rising edge on the data contact, the DS2890 waits (t_{PDH}, 15-60 µs at regular speed, 2-6 µs at Overdrive speed) and then transmits the Presence Pulse (t_{PDL}, 60-240 µs at regular speed, 8-24 µs at Overdrive Speed). A Reset Pulse of 480 µs or longer will exit the Overdrive Mode returning the device to regular speed. If the DS2890 is in Overdrive Mode and the Reset Pulse is no longer than 80 µs the device will remain in Overdrive Mode.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 15 (a-c). The master initiates all time slots by driving the data line low. The falling edge of the data line synchronizes the DS2890 to the master by triggering an internal timing circuit. During write time slots, the timing circuit determines when the DS2890 will sample the data line. For a read data time slot, if a “0” is to be transmitted, the timing circuit determines how long the DS2890 will hold the data line low. If the data bit is a “1”, the DS2890 will not hold the data line low at all.

Figure 14. **INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES"**



RESISTOR
MASTER
DS2890

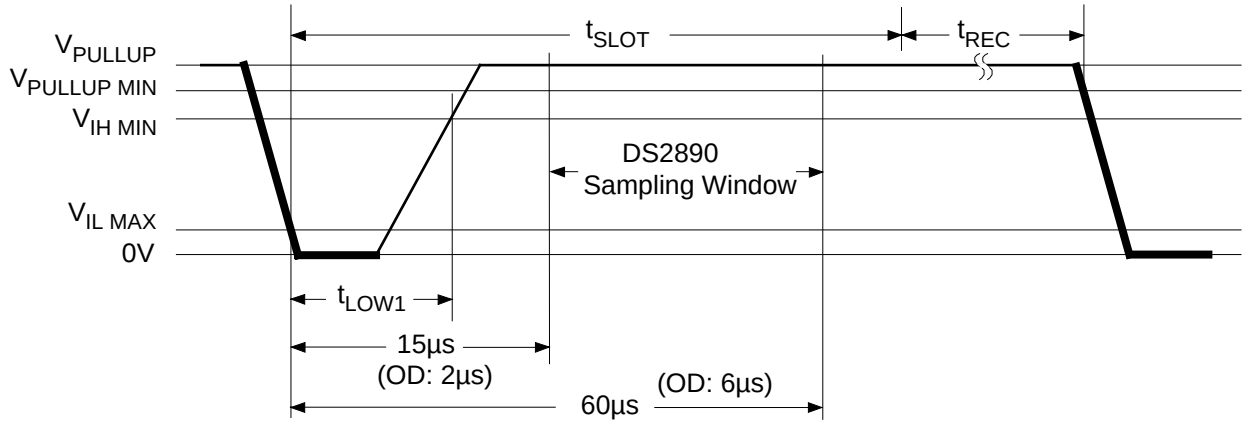
REGULAR SPEED	OVERDRIVE SPEED
480 µs ≤ t_{RSTL} < ∞*	48 µs ≤ t_{RSTL} < 80 µs
480 µs ≤ t_{RSTH} < ∞**	48 µs ≤ t_{RSTH} < ∞**
15 µs ≤ t_{PDH} < 60 µs	2 µs ≤ t_{PDH} < 6 µs
60 ≤ t_{PDL} < 240 µs	8 ≤ t_{PDL} < 24 µs

* In order not to mask interrupt signaling by other devices on the 1-Wire bus and to prevent a power-on reset of the parasite powered circuit, t_{RSTL} + t_R should always be less than 960 µs.

** Includes recovery time.

Figure 15. **READ/WRITE TIMING DIAGRAMS**

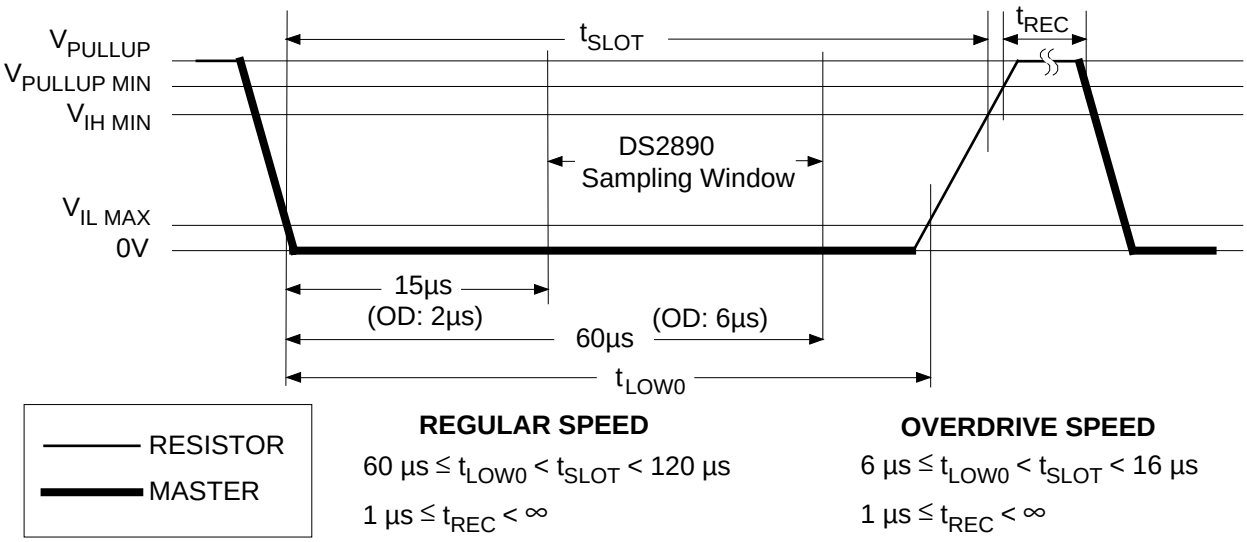
a) Write-one Time Slot



REGULAR SPEED	OVERDRIVE SPEED
60 µs ≤ t_{SLOT} < 120 µs	6 µs ≤ t_{SLOT} < 16 µs
1 µs ≤ t_{LOW1} < 15 µs	1 µs ≤ t_{LOW1} < 2 µs
1 µs ≤ t_{REC} < ∞	1 µs ≤ t_{REC} < ∞

RESISTOR
MASTER

b) Write-zero Time Slot



RESISTOR
MASTER

REGULAR SPEED

60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs

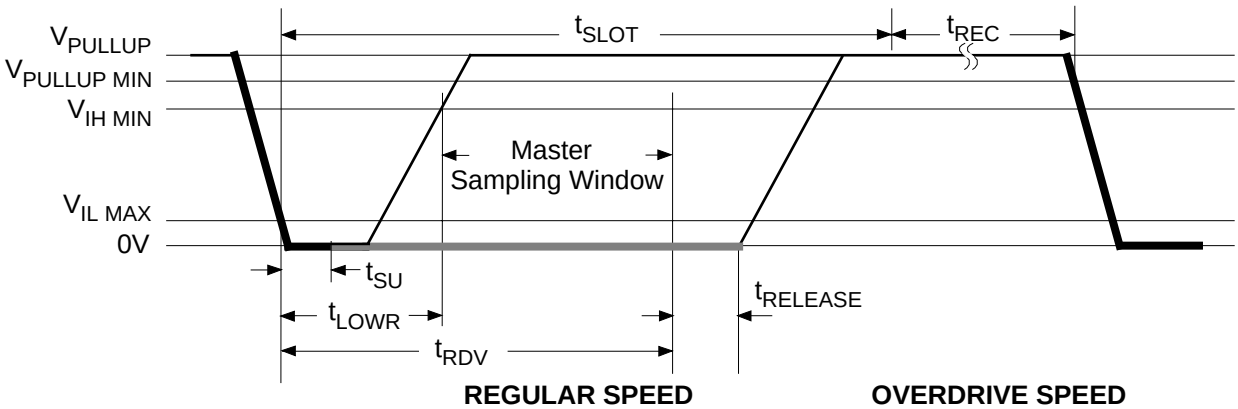
1 µs ≤ t_{REC} < ∞

OVERDRIVE SPEED

6 µs ≤ t_{LOW0} < t_{SLOT} < 16 µs

1 µs ≤ t_{REC} < ∞

c) Read-data Time Slot



RESISTOR
MASTER
DS2890

REGULAR SPEED

60 µs ≤ t_{SLOT} < 120 µs

1 µs ≤ t_{LOWR} < 15 µs

0 ≤ $t_{RELEASE}$ < 45 µs

1 µs ≤ t_{REC} < ∞

t_{RDV} = 15 µs

t_{SU} < 1 µs

OVERDRIVE SPEED

6 µs ≤ t_{SLOT} < 16 µs

1 µs ≤ t_{LOWR} < 2 µs

0 ≤ $t_{RELEASE}$ < 4 µs

1 µs ≤ t_{REC} < ∞

t_{RDV} = 2 µs

t_{SU} < 1 µs

*The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE}$ = 0).

Figure 16. **POTENTIOMETER FUNCTION COMMAND FLOW**

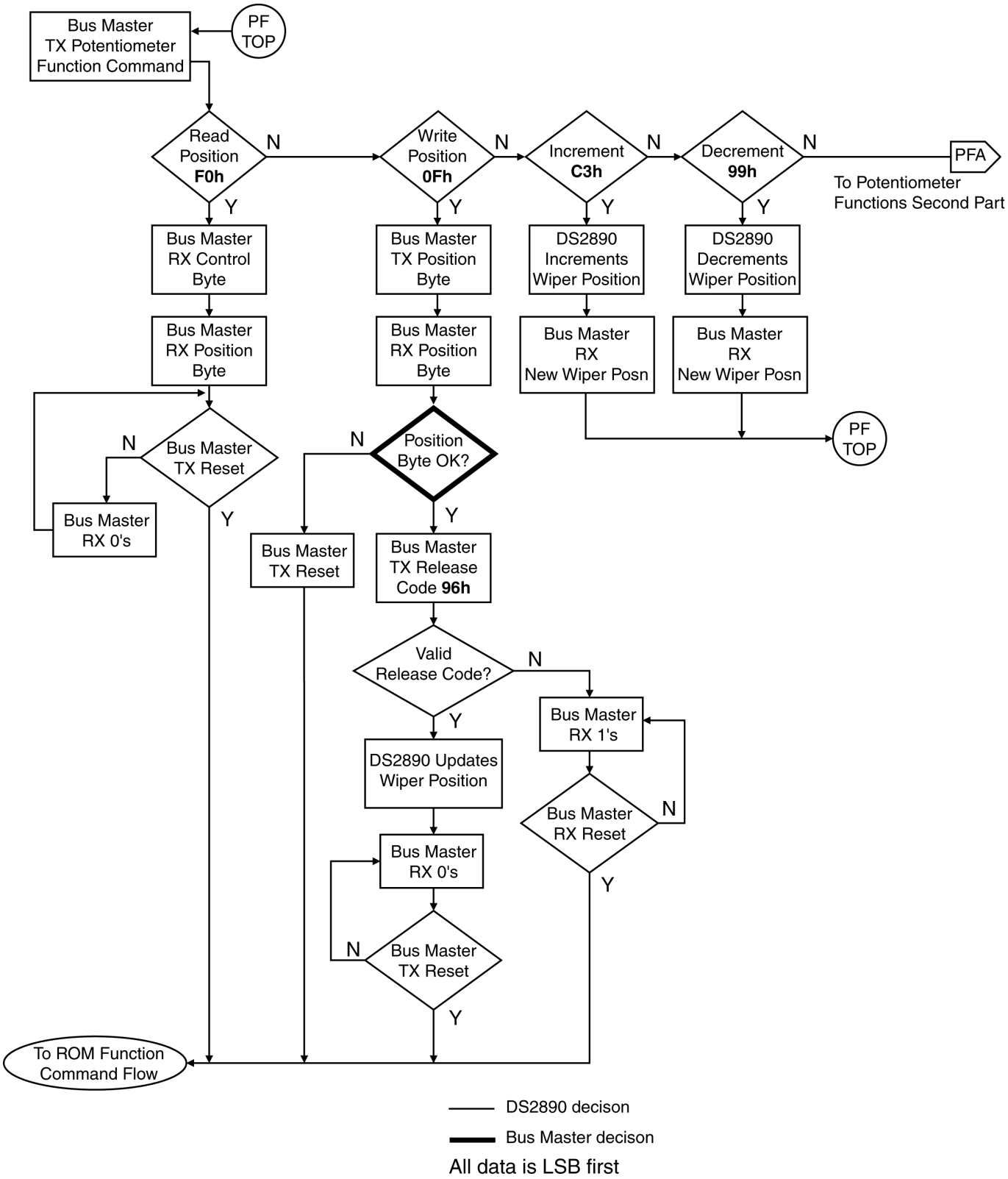
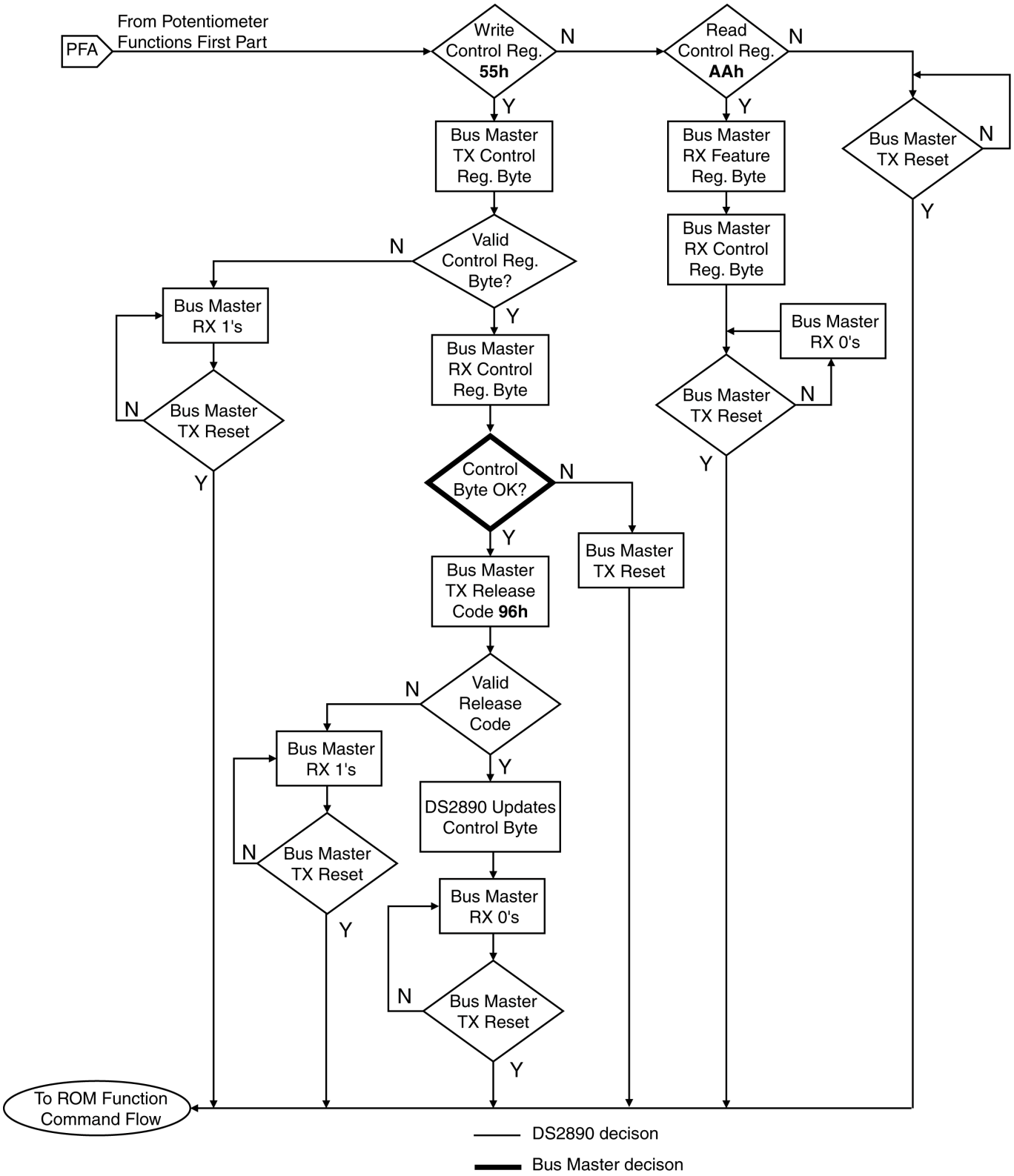


Figure 17. **POTENTIOMETER FUNCTION COMMAND FLOW** (continued)



All data is LSB first

Figure 18. **ROM FUNCTION COMMAND FLOW**

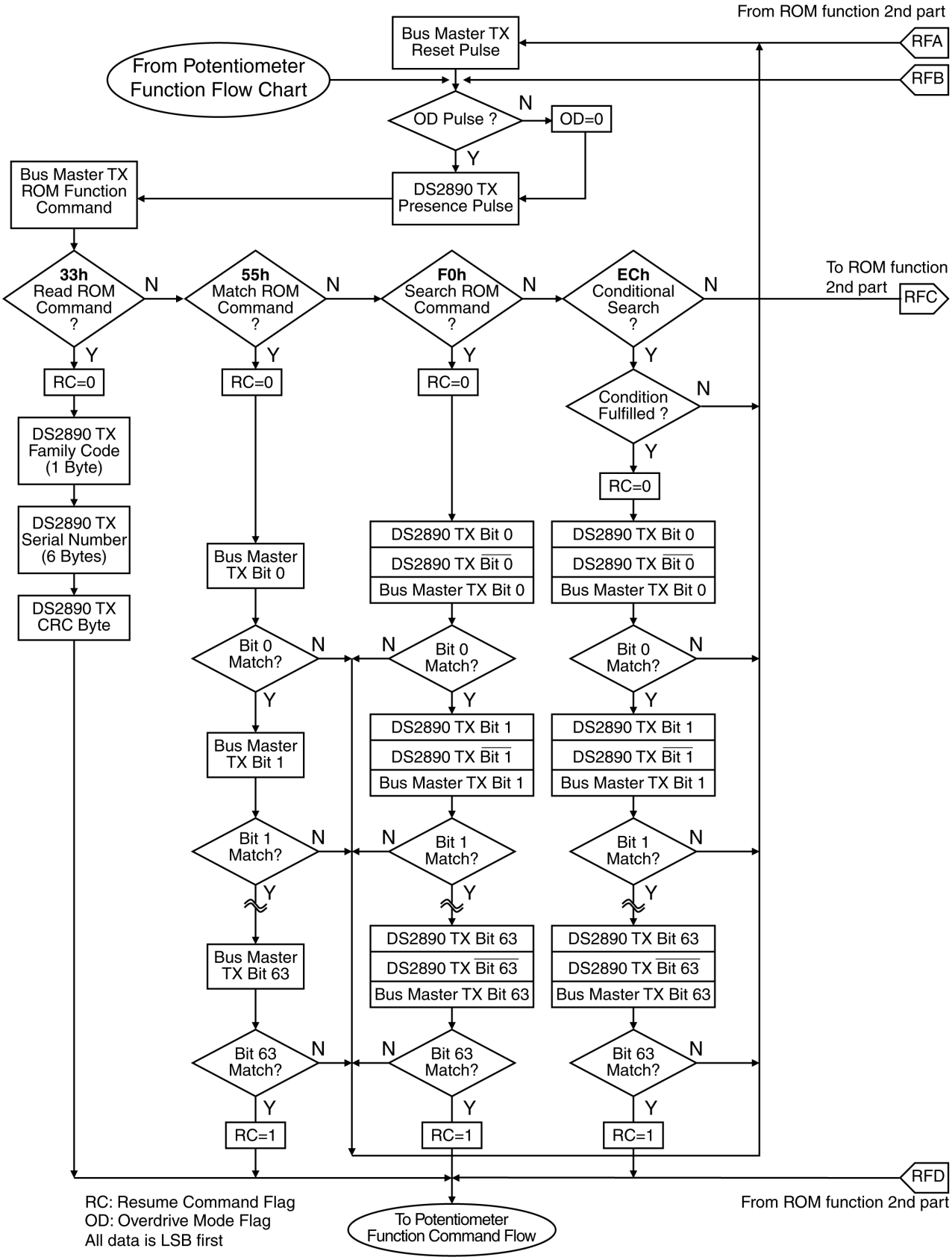
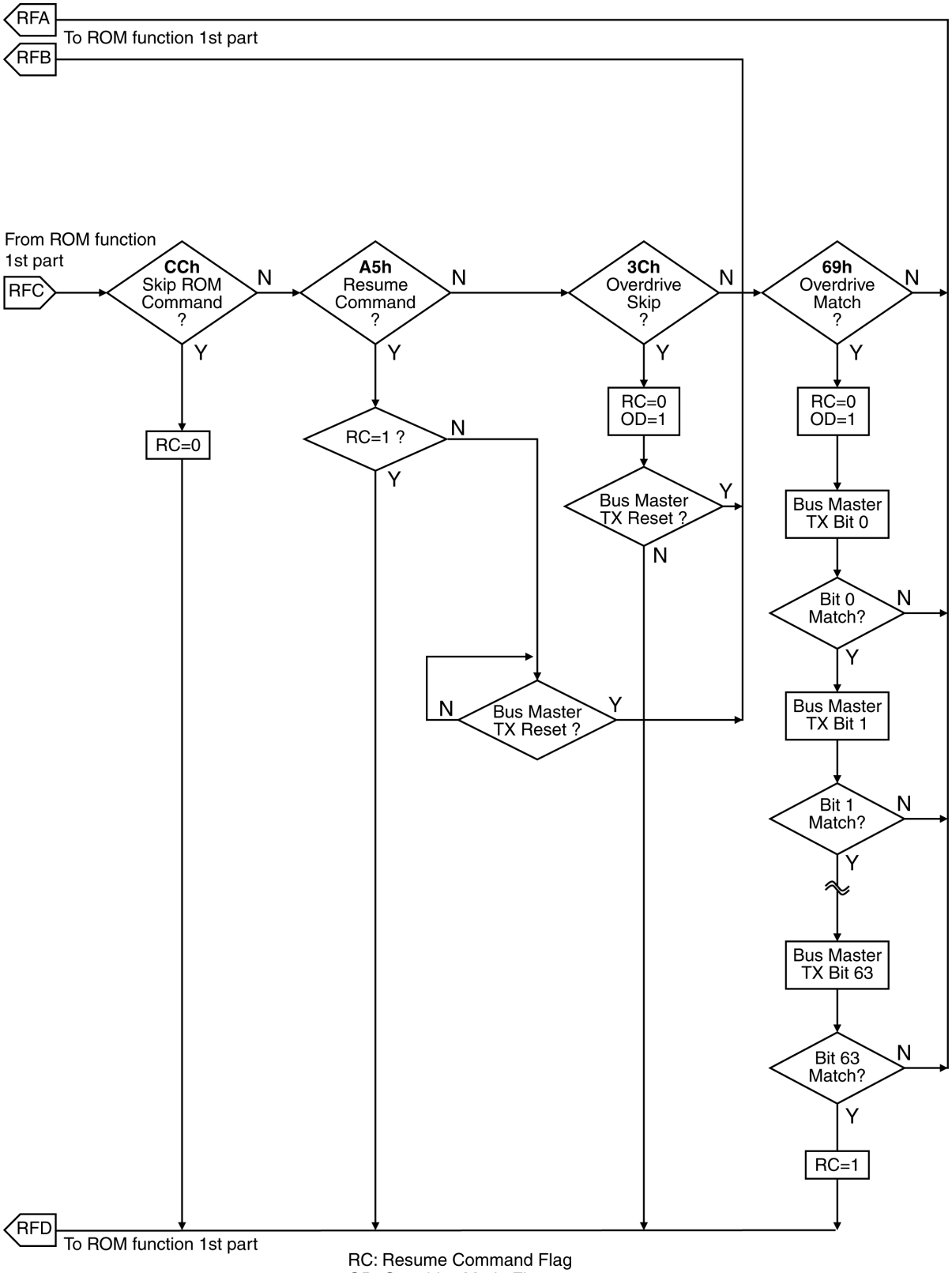


Figure 19. **ROM FUNCTION COMMAND FLOW** (continued)



RC: Resume Command Flag
OD: Overdrive Mode Flag
All data is LSB first

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage on RH, RL, WIPER Relative to Ground	-0.5V to +11.0V
Voltage on Other Pins Relative to Ground	-0.5V to +6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

$-40°C \le T_A \le +85°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Pull-Up Voltage	V_{PUP}	2.8		6.0	V	1
Auxiliary Supply Voltage	V_{DD}	2.8		6.0	V	1,2
		-0.3		0.8	V	1,3

NOTES:

1. Voltages are referenced to ground
2. Range applicable when an auxiliary V_{DD} supply is used
3. Range applicable when an auxiliary V_{DD} supply is not used

POTENTIOMETER CHARACTERISTIC

$2.8V \le V_{PUP} \le 6.0V$, $-40°C \le T_A \le +85°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Resistor Terminal Voltage		-0.3		11.0	V	1
End-to-End Total Resistance			100		kΩ	
End-to-End Resistance Tolerance		-25		25	%	2
Wiper Resistance:	R_{WIPER}					3
Absolute Linearity			±0.6		LSB	4
Relative Linearity			±0.25		LSB	5
-3 dB cutoff frequency	f_{CUTOFF}	100			kHz	
Temperature Coefficient			800		ppm/°C	

NOTES:

1. Voltage is referenced to ground.
2. Valid at 25°C only.
3. Wiper resistance is a function of operating characteristics. See section "POTENTIOMETER WIPER RESISTANCE AND CHARGE PUMP CONSIDERATIONS" for R_{WIPER} characteristics.
4. Absolute linearity is a measure of wiper output voltage versus expected wiper voltage as determined by wiper position.
5. Relative linearity is a measure of the output deviation between successive potentiometer tap points.

DC ELECTRICAL CHARACTERISTICS

$2.8V \leq V_{PUP} \leq 6.0V$, $-40°C \leq T_A \leq +85°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Input High	V_{IH}	2.2			V	1
1-Wire Input Low	V_{IL}	-0.3		0.8	V	1,2
1-Wire Output High	V_{OH}		V_{PUP}	6.0	V	1,3
1-Wire Output Low @ 4 mA	V_{OL}			0.4	V	1
1-Wire Input Leakage Current	I_L		5		µA	4
V_{DD} Input Current, Charge Pump OFF	I_{DD}			4.0	µA	5
V_{DD} Input Current, charge Pump ON	I_{DD}			2.0	mA	6

NOTES:

1. Voltages are referenced to ground.
2. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.
3. V_{PUP} is the external 1-Wire pull-up voltage.
4. Input load is to ground.
5. Input current when an auxiliary V_{DD} supply is used and the charge pump is turned OFF.
6. Input current when an auxiliary V_{DD} supply is used and the charge pump is turned ON.

AC ELECTRICAL CHARACTERISTICS - REGULAR 1-WIRE SPEED

$2.8V \le V_{PUP} \le 6.0V$, $-40°C \le T_A \le +85°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	
Read Data Valid	t_{RDV}		15		µs	1
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	2
Recovery Time	t_{REC}	1			µs	
Reset High Time	t_{RSTH}	480			µs	3
Reset Low Time	t_{RSTL}	480			µs	4
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1. The optimal sampling point for the master is as close as possible to the end time of the 15 µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE} = 0$).
2. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.
3. An additional reset or communication sequence cannot begin until the reset high time (t_{RSTH}) has expired.
4. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

AC ELECTRICAL CHARACTERISTICS - OVERDRIVE 1-WIRE SPEED

$2.8V \le V_{PUP} \le 6.0V$, $-40°C \le T_A \le +85°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	6		16	µs	
Write 1 Low Time	t_{LOW1}	1		2	µs	
Write 0 Low Time	t_{LOW0}	6		16	µs	
Read Low Time	t_{LOWR}	1		2	µs	
Read Data Valid	t_{RDV}		2		µs	9
Release Time	$t_{RELEASE}$	0	1.5	4	µs	
Read Data Setup	t_{SU}			1	µs	4

AC ELECTRICAL CHARACTERISTICS - OVERDRIVE 1-WIRE SPEED

$2.8V \le V_{PUP} \le 6.0V$, $-40°C \le T_A \le +85°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery Time	t_{REC}	1			µs	
Reset High Time	t_{RSTH}	48			µs	
Reset Low Time	t_{RSTL}	48		80	µs	
Presence Detect High	t_{PDH}	2		6	µs	
Presence Detect Low	t_{PDL}	8		24	µs	

NOTES:

1. The optimal sampling point for the master is as close as possible to the end time of the 2 µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE} = 0$).
2. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge.
3. An additional reset or communication sequence cannot begin until the reset high time (t_{RSTH}) has expired.
4. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

CAPACITANCE

TA = 25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Pin				800	pF	1
V_{DD} Pin			10		pF	
Resistor Terminals				10	pF	

NOTE:

1. Capacitance on the 1-Wire pin could be 800 pF when power is first applied. If a 5 kΩ is used to pull up the 1-Wire line to V_{PUP}, the capacitance will not affect communications after a 5 µs charge time.

DS9097/DS9097E
COM Port Adapter

www.dalsemi.com

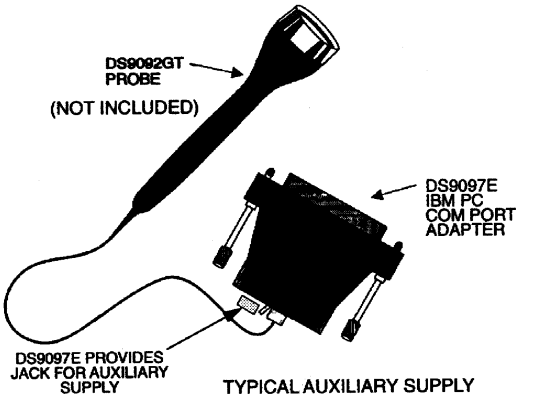
FEATURES

- Provides a simple, low-cost interface to an RS232C COM Port for reading and writing iButton™ devices (DS9097E required for programming DS198x Add-Only iButtons)
- Adapter is powered entirely from an RS232 interface (DS9097E may require optional auxiliary 12V supply)
- Standard DB-9 (DSD9097) or DB-25 (DS9097E) female connector for mating the adapter to the COM Port of a computer and RJ-11 connector for easy attachment of a probe such as the DS9092GT
- DS9097E has an additional 2.1 mm male power jack to allow for an auxiliary 12V DC supply for programming Add-Only iButtons

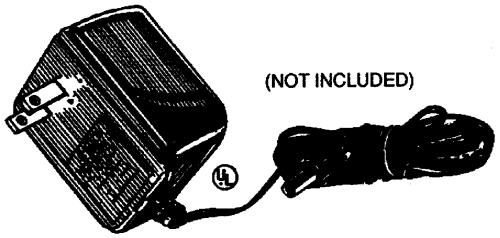
  Pin assignment DS9097, DB-9
  TXD (3), RXD (2), DTR (4), PC-Ground (5); all other pins not connected

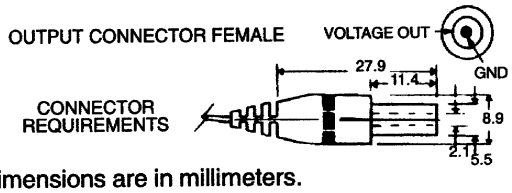
  Pin assignment DS9097E, DB-25
  TXD (2), RXD (3), DTR (20), RTS (4), PC-Ground (7); all other pins not connected

  Auxiliary supply should be a regulated 12V @ 10 mA minimum, center=GND, outer ring=V+ (Newark Electronics Stock No. 84F2081, Allied Electronics Stock No. 928-9895, Stancor Model STA-300R, or equivalent)



TYPICAL AUXILIARY SUPPLY





All dimensions are in millimeters.

DESCRIPTION

The DS9097 COM Port Adapter is a simple, low-cost passive adapter which performs RS232C (±12V) level conversion, allowing an iButton probe to be connected to the serial port of a computer so that a non-EPROM iButton can be read and written directly. It can also read all EPROM-based iButtons. The serial port must support a data transmission rate of 115.2 kbits/s in order to create the 1-Wire™ time slots correctly. Nearly all PCs support the required data rate and are fully compatible with the DS9097. Since an 8-bit character (6 data bits plus start and stop bit) on the RS232 port operating at 115.2 kbits/s is used to form a single 1-Wire time slot, the maximum effective 1-Wire transfer rate is 14.4 kbits/s (regular speed). Details on the operation of the DS9097 including software examples are found in Application Note 74, Section V.

The DS9097E is an upgraded version of the DS9097 that is capable of supplying the 12 volts necessary to program the EPROM-based iButton products (DS198x Add-Only iButtons) in addition to reading and writing SRAM and EEPROM-based devices (DS199x, DS196x, DS197x). When combined with the appropriate software, the DS9097E can be used in a standalone mode where all of the programming current is supplied by the serial port itself. In this configuration, the maximum number of EPROM bits that can be programmed simultaneously is four on a typical serial port. For higher performance, the above mentioned 12V auxiliary supply can be plugged into the power jack on the DS9097E and with proper software enable the serial port to program up to eight EPROM bits simultaneously.